WORLD BANK GROUP

FORGING VIET NAM'S SEMICONDUCTOR FUTURE

A tech talent and innovation flywheel

特别提醒

行业交流分享群

分享：可获取人资行业的报告、方案及其他学习资源，上新群内通知

交流：求职、找人、找资源、找供应商

客服

交流群

免责声明

第三方声明：本报告所有内容（数据/观点/结论）整理于网络公开渠道，均不代表我司立场，我司不承担其准确性、完整性担保责任。

侵权处理承诺：如报告内容涉嫌侵权，请立即联系客服微信，我司将在核实后第一时间清理相关内容并配合处理

1818 H Street NW
Washington DC 20433
Telephone: 202-473-1000
Internet: www.worldbank.org

Cover design: Ha Doan & Duong Phan

WORLD BANK GROUP

FORGING VIET NAM'S SEMICONDUCTOR FUTURE

A tech talent and innovation flywheel

CONTENTS

BOXES

FIGURES

TABLES

Acronyms

AI	Artificial Intelligence
ASIC	Application-Specific Integrated Circuit
AP	Advanced Packaging
ATP	Assembly, Testing & Packaging
AVSE	Association of Vietnamese Scientists and Experts
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
BK21	Brain Korea 21
CAD	Computer-Aided Design
CMOS	Complementary Metal-Oxide Semiconductor
CoE	Center of Excellence
CSE	Computer Science Engineering
DFC	Double First Class
E&E	Electronics and Electrical Equipment
EDA	Electronic Design Automation
EDB	Economic Development Board
EE	Electrical Engineering
ERP	Enterprise Resource Planning
ESG	Environmental, Social, and Governance
EU	European Union
EV	Electric Vehicle
FDI	Foreign Direct Investment
FEF	Faculty Excellence Fund
FPGA	Field-Programmable Gate Array
GDP	Gross Domestic Product
GPU	Graphics Processing Unit
GVC	Global Value Chain
HCMUS	University of Science (Vietnam National University Ho Chi Minh City)
HCMUT	University of Technology (Vietnam National University Ho Chi Minh City)
HE	Higher Education
HPC	High Performance Computing
HUST	Hanoi University of Science and Technology
HVAC	Heating, Ventilation, And Air Conditioning
IC	Integrated Circuit
ICT	Information and Communication Technology
INOMAR	Center for Innovative Materials and Architectures (Vietnam National University Ho Chi Minh City)
INT	Institute for Nanotechnology (Vietnam National University Ho Chi Minh City)
IoT	Internet of Things
IP	Intellectual Property
IPP	Industry Postgraduate Programme
ISF	Investment Support Fund
IT	Information Technology
ITRI	Industrial Technology Research Institute
KAIST	Korea Advanced Institute of Science and Technology
KIPO	Korean Intellectual Property Office
KPI	Key Performance Indicator
LDO	Low Dropout Regulator
LFS	Labor Force Survey
LLM	Large Language Model
MEMS	Micro-Electro-Mechanical Systems
MES	Manufacturing Execution System
MIDA	Malaysia's Industrial Development Authority
ML	Machine Learning
MNC	Multinational Corporation
MOET	Ministry of Education and Training
MOF	Ministry of Finance
MOIT	Ministry of Industry and Trade
MOSIS	Metal Oxide Semiconductor Implementation Service

MOST	Ministry of Science and Technology
MPW	Multi-Project Wafer
MSc	Master of Science
MSCA	Marie Sklodowska-Curie Actions
NAFOSTED	National Foundation for Science and Technology Development
NIC	National Innovation Center
NPSTID	National Program on Strategic Technology & Industry Development
NSTIC	National Semiconductor Translation & Innovation Centre
OECD	Organisation for Economic Co-operation and Development
OPEX	Operational Expenditure
OSAT	Outsourced Semiconductor Assembly and Test
PACT	Partnerships for Capability Transformation
PCB	Printed Circuit Board
PCP	Professional Conversion Program
PhD	Doctor of Philosophy
PLL	Phase-Locked Loop
PPP	Public-Private Partnership
PVD	Physical Vapor Deposition
R&D	Research and Development
RF	Radio Frequency
RIE2025	Research, Innovation, and Enterprise 2025 (Singapore)
RTL	Register Transfer Level
S&E	Science and Engineering
S&T	Science and Technology
SCOPUS	Elsevier's abstract and citation database
SgIS	Singapore Industry Scholarship
SIDIF	Strategic Industry Development Investment Fund
SiP	System in Package
SME	Small and Medium-sized Enterprise
SMT	Surface-Mount Technology
SoC	System on Chip
SSIA	Singapore Semiconductor Industry Association
STEM	Science, Technology, Engineering, and Mathematics
STI	Science, Technology, and Innovation
TSMC	Taiwan Semiconductor Manufacturing Company
TSRI	Taiwan Semiconductor Research Institute
TTO	Technology Transfer Office
TVET	Technical and Vocational Education and Training
TWAREN	TaiWan Advanced Research and Education Network
UD	University of Da Nang
UIT	University of Information Technology (Vietnam National University Ho Chi Minh City)
US	United States
UVM	Universal Verification Methodology
VinaREN	Viet Nam's National Research and Education Network
VITALS	Vietnam Innovation & Talent Alliance for Semiconductors
VLSI	Very-Large-Scale Integration
VNEI	Viet Nam Network of Higher Education Innovation and Entrepreneurship Centers
VNU	Vietnam National University
VNUHCM	Vietnam National University Ho Chi Minh City
VNUHN	Vietnam National University, Hanoi
VSRI	Viet Nam Semiconductor Research Institute
VUDP	Viet Nam University Development Project
WIPO	World Intellectual Property Organization
WLCSP	Wafer-Level Chip Scale Packaging
WB	World Bank

Acknowledgements

This report is a collective endeavor and involved several parts of the Bank including EDU, DD, FCI, and EAPCE, and a deliverable for the "Viet Nam's Skilled Workforce Development for a Tech-intensive Economy" ASA.

The report was authored by Nguyet Anh Tran (Economist), Ekua Bentil (Senior Education Specialist), and Trang Hong Dao (Consultant). The following core team members co-authored background assessments, reviewed and provided substantive inputs to this report: Dung Kieu Vo (Senior Education Specialist), Huong Lan Thi Tran (Senior Digital Development Specialist), Johan Bjurman Bergman (Digital Development Specialist), Mike Nguyen (Senior Industry Consultant), Vinh Quang Dang (Senior Private Sector Specialist), Gu-Yeon Wei (Robert and Suzanne Case Professor, Harvard University), and Joshua Park (Consultant).

The report diagnosis drew significantly from the following background papers and technical notes:

1. Viet Nam semiconductor industry rapid assessment, by Mike Nguyen, Huong Lan Thi Tran, and Johan Bjurman Bergman.

2. Skilling up for Viet Nam's semiconductor industry: Assessing talent gaps and higher education capacity, by Trang Hong Dao, Ekua Bentil, Gu-Yeon Wei, Dung Kieu Vo, Joshua Park, and NguyetAnh Tran.

3. Promoting university R&D and technology transfer for productivity growth in Viet Nam, by Vinh Quang Dang, Cristian Quijada Torres, Kibum Kim, NguyetAnh Tran, and Dinh Tuan Minh.

4. Roles of Viet Nam National University, Ho Chi Minh City in advancing Viet Nam's Semiconductor Vision: A rapid infrastructure review and policy recommendations, by Ekua Nuama Bentil, Gu-Yeon Wei, Dung Kieu Vo, and Joshua Park.

5. Equitable financing for Viet Nam's STEM higher education, by NguyetAnh Tran and Trang Hong Dao.

The team is grateful for valuable contributions at various stages from the World Bank and IFC colleagues: Omar Arias (Lead Economist), Diego Ambasz (Senior Economist), Mira Nahouli (Senior Operations Officer), Ridhi Gupta (Investment Officer), Abla Safir (Senior Economist), Sacha Dray (Economist), Juliana Guaqueta Ospina (Senior Education Specialist), and Dung Viet Do (Senior Country Officer).

The team greatly benefited from inputs, discussions, and reviews provided by Vietnamese university leaders and government agencies: Assoc. Prof. Vu Hai Quan (Chancellor, Viet Nam National University Ho Chi Minh City – VNUHCM), Prof. Le Quan (President, Viet Nam National University, Hanoi), Assoc. Prof. Huynh Quyet Thang (President, Hanoi University of Science and Technology), Mr. Do Tien Thinh (Deputy Director General, National Innovation Center), and from VNUHCM – Dr. Bui Thi Hong Hanh (Director of External Affairs), Assoc. Prof. Nguyen Luu Thuy Ngan (Rector, University of Information and Technology –UIT), Assoc. Prof. Pham Tran Vu (Rector, University of Technology – HCMUT), Assoc. Prof. Huynh Phu Minh Cuong (Vice Dean, UoT), and Assoc. Prof. Trinh Le Huy (UIT). The team especially thanks VNUHCM for their support in facilitating and co-organizing multiple site visits, data collection, and the report consultation workshop in VNUHCM.

We thank participants from the semiconductor industry and overseas universities for their inputsand comments, in particular, Dr. Aaron Thean (Vice President & Provost, National University of Singapore – NUS), Dr. Vu Minh Khuong (Professor, NUS), Dr. Kee-won Kwon (Professor, Sungkyunkwan University), Jeff Goss (Arizona State University), Kenneth Tse (General Director, Intel Viet Nam), Kevin Koh (President, Faraday Technology Vietnam), and Tran Dac Khoa (General Director, Renesas Design Viet Nam), and Duy Tan Tran (President, Savarti Inc.).

Financial support from Australian Aid is gratefully acknowledged for the background assessment on financing for Viet Nam's STEM higher education.

The team is grateful for the overall guidance from Mariam J. Sherman (Division Director, Viet Nam, Cambodia, and Lao PDR) and Cristian Aedo (Practice Manager, Education East Asia & Pacific). The report benefited from comments from World Bank Peer Reviewers: Alex Twinomugisha (Senior Education Specialist), Marina Bassi (Program Leader), Cristian Quijada Torres (Senior Private Sector Specialist), Hania Kronfol (Senior Digital Development Specialist), and Sandra Sargent (Senior Digital Development Specialist).

The report was assisted by Van Cam Nguyen (Program Assistant) and designed by Ha Doan (Consultant).

Scope note

Why this report? Viet Nam has prioritized semiconductors as one of ten critical technologies and set explicit goals of becoming a global semiconductor talent hub by 2030, moving up the value chain toward higher value-added segments, and developing a complete semiconductor value chain by 2045. Delivering on that pledge hinges on strategic and urgent investment in top talent, science, and innovation.

Scope & Exclusions: This report concentrates on the most urgent gap cultivating a cadre of scientists and engineers (S&E) and, to the extent possible, tech entrepreneurs to support Viet Nam s semiconductor and high-tech ambitions. The analysis and interventions focus on the highly skilled workforce and frontier talent development, and cover research, innovation, and university-industry linkages in relation to the talent challenges.

The report recognizes that to unlock its semiconductor potential, Viet Nam must address other binding constraints, notably: weak linkages between FDI and domestic firms, emerging infrastructure gaps (e.g., energy and logistics), and intellectual property rights regulations, amid evolving geoeconomic conditions. We also acknowledge the critical role of technicians, especially those with technical degrees, in the assembly, test, and packaging segment where Viet Nam has a strong presence. However, given the scope of this report, these topics are referenced only where they directly relate to the report s focus.

Complementary Reports, Policy Notes and Technical Assessments

The report draws on broader World Bank research on Viet Nam s structural transformation, including Viet Nam 2045: Trading Up in a Changing World (World Bank, 2024a) the flagship report that frames value chain upgrading as a pathway to high-income status, identifies economy-wide challenges, opportunities and policy options. Improving the Performance of Higher Education in Viet Nam: Strategic Priorities and Policy Options (World Bank, 2020b) and Higher Education Financing in Viet Nam (World Bank, 2023a) provides a sectoral review of Viet Nam s higher education system.

Deep-diving assessments on key thematic areas of this report could be found in five technical and policy notes. (1) Viet Nam Semiconductor Industry Rapid Assessment (Nguyen, Tran, and Bergman, 2025) maps firm-level capabilities and market opportunities, identifying three upgrading industry opportunities across design and manufacturing. (2) Skilling up for Viet Nam' s semiconductor industry (Dao et al., 2025) quantifies the demand-supply mismatches for skilled workers and higher education system capacity gaps under alternative upgrading scenarios. (3) Role of Viet Nam National University, Ho Chi Minh City in advancing Viet Nam' s Semiconductor Vision (Bentil et al., 2025) deep dives into the infrastructure conditions and investment needs for training and research, and international good practices in VNUHCM. (4) Promoting University R&D and Technology Transfer for Productivity Growth in Viet Nam (Dang et al., 2025) provides a system diagnostics of university R&D and proposes legal and institutional reforms to strengthen university-led research and technology. (5) Equitable financing for Viet Nam' s STEM higher education (Tran and Dao, 2025) assesses affordability and equity of STEM higher education that supports Vietnam' s ambition to grow its high-tech and high value-added manufacturing base.

EXECUTIVE SUMMARY

A dynamic tech talent and innovation flywheel

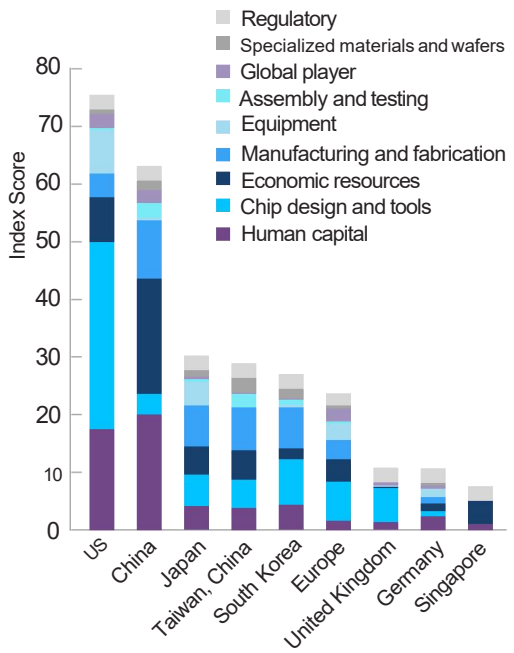
The world is entering an artificial intelligence (AI)-driven semiconductor supercycle, with unprecedented demand for chips powering everything from generative AI to electric vehicles. Global semiconductor sales are projected to double this decade – surpassing US$1 trillion by 2030. This AI supercycle could generate an estimated US$15 trillion in economic output and 100 million jobs by 2030 across all sectors – if the tech infrastructure can keep up. National strength in domains such as AI and semiconductors hinges on three foundational pillars: superior innovation ecosystems, human capital, and economic resources.

AI and semiconductors are at the very core of the global technological convergence. Technology convergence is accelerating across the tech stack of five of the most critical and emerging technologies – AI, semiconductors, biotech, space, and quantum – in which advancements in one domain create network effects that spur progress in others, often in unpredictable ways.

Figure ES-1. East Asia: Global Top 100 Science and Tech clusters

Source: WIPO 2024

Figure ES-2. Semiconductor technology index by economies and foundational pillars

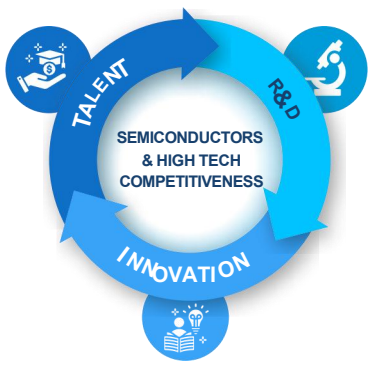


Source: Harvard's Belfer Center Critical and Emerging Technologies Index 2025 – Semiconductor Index Ranking.

Viet Nam is right at the heart of a global semiconductor cluster. Global evidence is clear: firms set up R&D-intensive activities in locations where cutting-edge talent and research co-locate with ready infrastructure. Five East Asian economies – China, South Korea, Japan, Singapore, and Taiwan (China) – rank among the global leaders in both AI and semiconductor technologies. These economies now host the world's five largest science and technology clusters and 35 of the global top 100 (with Malaysia contributing one cluster as of 2024). All of them have fused human capital development policy with long-term, aggressive investment in mission-driven research and innovation – vaulting from technology assembly and manufacturing bases to knowledge- and tech-intensive economies.

The clock for Viet Nam's talent investment is already ticking. A global semiconductor workforce shortfall – ranging from tens to hundreds of thousands in leading economies by 2030 – demonstrates that fabs and tax breaks alone cannot sustain an ecosystem. For Viet Nam, the country already possesses two critical assets: a growing tech talent pipeline and top-level political commitment. Yet, entrenched constraints in advancing the skills base, nurturing and retaining frontier talent, and building innovation capacity and infrastructure threaten to stall progress.

Figure ES-3. A talent, R&D, and innovation flywheel



This report envisions a talent, R&D, and innovation flywheel that produces a high-quality semiconductor workforce and drives innovation to realize Viet Nam's semiconductor ambitions. A successful semiconductor ecosystem rests on three foundational pillars: advanced chip design know-how, sustained capital investment, and a critical mass of highly skilled human capital – with talent development as the critical lever across all three.

This report proposes that Viet Nam must integrate its workforce development, higher education, and innovation ecosystems so that the government, universities, and industry can reinforce each other in cultivating a deep, expansive talent pool, driving research and innovation, and propelling the country up the value chain – for the semiconductor and other technology-intensive industries.

To act with speed and scale, four mutually reinforcing pillars are proposed:

1. Ignite Talent – expand and deepen the skilled workforce, and nurture a frontier tech talent pipeline.
2. Build Shared Training and R&D Infrastructure – give students and universities access to industry-standard tools, facilities and infrastructure.
3. Catalyze University-Industry Innovation – turn research into marketable designs, products and solutions.
4. Govern & Finance for Results – lock in accountability and sustained funding.

Investing in tech talent can pay economy-wide dividends – creating tens of thousands of high-paying jobs and boosting other high-tech sectors. A larger, more skilled workforce also enables local firms to move up the value chain and attracts higher-quality foreign direct investment (FDI), creating a virtuous cycle. Lastly, breakthroughs in chips generate network effects, catalyzing progress in strategic technologies such as AI, biotech, and space. The milestones are clear. By 2035, Viet Nam should aim to be recognized as a global semiconductor talent hub – with a self-sustaining pipeline, vibrant domestic chip design houses, and the credibility to attract the next wave of investment.

The window to deliver these outcomes is narrow - but still open. Regional peers and aspirants such as Malaysia, Singapore, and China are already expanding rapidly in cutting-edge semiconductor areas. Viet Nam urgently needs to address its talent shortfall in order to compete. While such bold actions present challenges, these can be effectively mitigated. Acting decisively now will determine whether Viet Nam shapes – or merely observes – the future of advanced industry in the region.

No country has ever suffered from having "too many" quality talent - but many have lost out by having too few.

Viet Nam's semiconductor moment: Moving up the ladder

A confluence of factors makes Viet Nam's ambitious semiconductor vision timely: its young and technically skilled workforce, the government's prioritization of innovation, and mounting interest from global tech firms. Many of these firms are already present or expanding in Viet Nam, drawn by an enabling environment primed for innovation-led growth – thanks to a suite of new supportive laws and funding programs.

Table ES-1. Readiness and intensity of potential gaps for Viet Nam's semiconductor upgrade pathways

Industry window	Viet Nam readiness 2024*	Knowledge / Talent intensity	Technology intensity	Capital intensity
Consolidate assembly, testing & packaging base	●●●●○ (4/5)	●○○○○ (1/5)	●○○○○ (1/5)	●●●○○ (3/5)
Expand back-end design services	●●○○○ (2/5)	●●●○○ (3/5)	●●●○○ (3/5)	●○○○○ (1/5)
Move into front-end IC design	●○○○○ (1/5)	●●●●● (5/5) ★	●●●●● (5/5)★	●●●●○ (4/5) ★
Leapfrog to advanced packaging	●○○○○ (1/5)	●●●●○ (4/5)	●●●●○ (4/5)	●●●●● (5/5) ★

* Viet Nam readiness 2024: composite score for current workforce, R&D capability and industrial base.
★ High fiscal-risk cells – large public funding requirement; PPPs or risk-sharing mechanisms recommended.

Viet Nam can pursue three strategic upgrade pathways, building on its existing strengths in back-end manufacturing (ATP – Assembly, Testing, Packaging) and growing capacity in back-end design services:

- Expand back-end design services: Viet Nam can grow as a hub for outsourced back-end design, particularly in layout and verification services. The number of IC design houses (around 40 today) could potentially double within five years, creating thousands of new engineering jobs. This segment has moderate knowledge intensity and can scale relatively quickly if the right skills are developed.
- Move into advanced packaging: Viet Nam could leapfrog into advanced packaging (e.g., 2.5D/3D chip stacking and System-in-Package (SiP) technologies) by leveraging early investments. Intel Viet Nam's pilot 3D packaging line and Amkor's new SiP facility already give Viet Nam a first-mover edge in the region. Advanced packaging is both technology- and capital-intensive, but it could become a niche specialization in which Viet Nam stands out.
- Leapfrog to front-end design: Developing indigenous chip intellectual property (IP) and full system-on-chip products would yield high-value design jobs and royalty streams. This path is highly knowledge-intensive, requiring top engineering and science talent (often with postgraduate degrees) to design and architect complex chips.

These three upgrading "windows" are mutually reinforcing, not mutually exclusive. Expanding Viet Nam's already solid foothold in back-end manufacturing, for example, could generate large-scale employment and industrial capability – thereby enabling a transition to higher-value segments like advanced packaging.

At the same time, Viet Nam also needs to consolidate its existing base in ATP. The country already has a solid foothold in back-end manufacturing with large investors like Intel and Amkor. Expanding existing plants and attracting new ones could add tens of thousands of skilled jobs by 2030, anchoring a local supply chain. Equally important, a strong ATP base generates large-scale employment and builds essential industrial know-how, which serves as a springboard to higher-value activities such as advanced packaging.

The connecting factor in all these cases is talent, R&D, and innovation: the more Viet Nam can acquire and develop talent, the greater its agility across the semiconductor value chain.

Semiconductor talent challenges: Extensive, intensive, and integrative margins

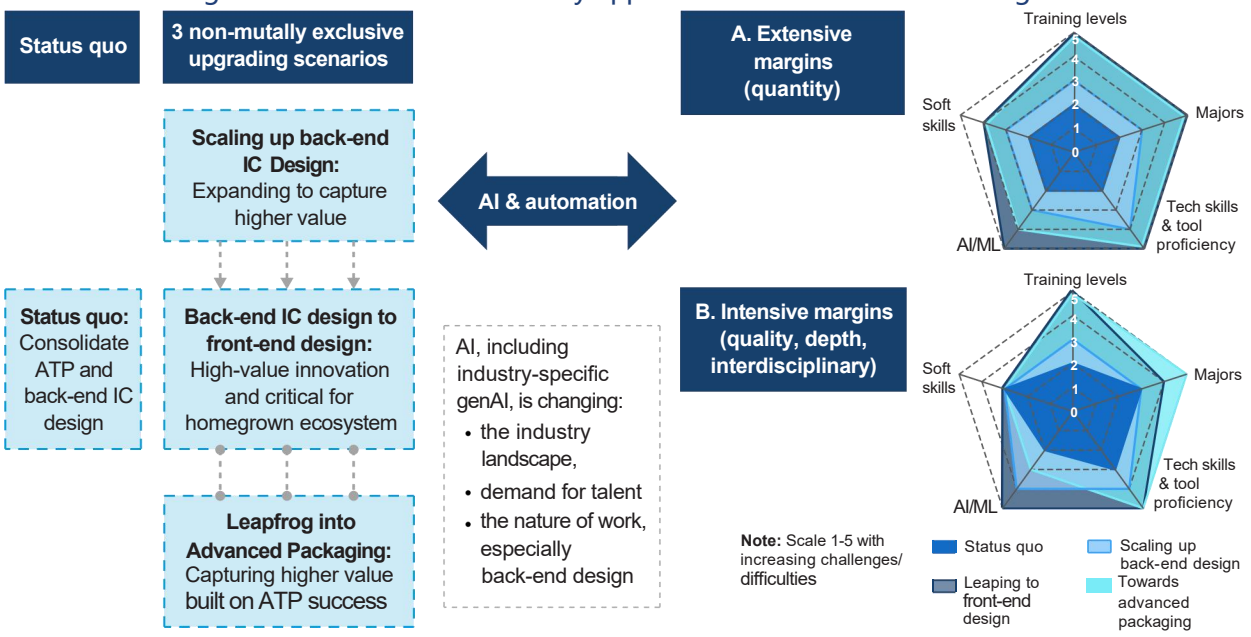
Positives regarding Viet Nam's talent pool certainly exist. Enrollments in science and engineering fields are rising by about 9 percent annually, for instance. Its top universities are also gaining regional recognition in the fields of science, technology, engineering, and mathematics (STEM). Currently, the country has over 500,000 professionals in their twenties and thirties with STEM degrees, with a further 24,000 projected to join the workforce each year.

If Viet Nam's semiconductor aspirations are translated into concrete actions that address identified gaps, it will vastly increase talent needs on:

- Extensive margins – quantity of skilled workers and frontier tech talent;
- Intensive margins – quality, depth, and interdisciplinarity, and with future-proof skill sets;
- Integrative margins – training-to-work, lab-to-fab, R&D-integrated training.

Future-Proof: Compounding the challenge is the fast-evolving nature of AI and interlocked technologies. AI is reshaping the industry, with the race for more powerful AI capabilities driving demand for advanced chips. It is also transforming the nature of demand for skills and intensifying the talent challenge. AI-powered design tools, for example, are automating certain routine chip design tasks and may reduce the need for entry-level back-end designers. At the same time, AI is increasing demand for engineers with expertise in cutting-edge areas such as machine learning and data science, and with the ability to solve complex edge-case problems.

Figure ES-4. Viet Nam's industry opportunities and the talent challenges



Quantity: Viet Nam s talent pool currently lacks what it needs to succeed in its semiconductor industry upgrade. In the country s strong assembly and testing segment, for example, only around 8 percent of workers in electronics factories hold a university degree; yet nearly half of current job postings in that segment require a bachelor s degree or higher. Scaling up back-end chip design activities would require tens of thousands of additional engineers beyond the current supply.

Quality & Depth: Moving into front-end design requires computer architects, chip designers, and other kinds of specialists with advanced degrees. Such talent is extremely scarce in Viet Nam; only around 4 percent of the current semiconductor workforce has a postgraduate degree, compared to around 30 percent in leading hubs. Advanced packaging operations present the same dilemma, with rising demand for expertise in materials science, chemistry, physics, and reliability engineering.

Integration: Meeting the fast-evolving technology cycles of the semiconductor industry is not just a question of improving skills in the abstract. To remain relevant and innovative, specialists must be tapped into the latest market trends and developments. At present, talent development takes place too far from the industry frontline. Breaking down existing silos between the education sector and business is therefore essential.

The multifold challenges of quantity, quality and depth, and integration in talent development underscore the urgency of immediate action. Viet Nam cannot rely on incremental improvements while others are already making bold, decisive moves.

Five critical decisions for 2025

Viet Nam has articulated a bold vision; 2025 is the year to pivot from planning to action. To kick-start the talent drive, five critical decisions are recommended for immediate implementation. Each decision is achievable within a year and aligns with the long-term pillars of the semiconductor ecosystem namely, human capital, technology, and investment.

- Decision 1: Fast-track a Semiconductor Graduate Fellowship (M.Sc./Ph.D.) Program. A national "Semiconductor Fellowship" program would fund full graduate scholarships for talented students to attend top-tier programs (abroad or in Viet Nam), creating a pipeline of tech talent and future faculty. Fellows would be bonded to return and work in Viet Nam through binding agreements and incentives.

  2025 action: Secure dedicated funding and launch the call for applications for the first cohort of fully funded semiconductor M.Sc./Ph.D. scholarships.

- Decision 2: Launch a "Faculty Excellence Fund." Establish a competitive program to build up Viet Nam s teaching and research faculty in critical semiconductor-related disciplines by: sponsoring early-career Vietnamese lecturers to pursue PhDs or postdoctoral training abroad; attracting top Vietnamese diaspora or foreign experts to teach in Viet Nam; and providing grants for lab setup and research upon their return.

  2025 action: Allocate funding starting in 2025 to support at least 50+ new faculty PhD scholarships (domestic or overseas) and initiate the hiring of 40+ international experts in key fields into universities.

- Decision 3: Create a national "EDA Cloud" platform. Provide centralized, low-cost access to industry-standard chip design software (Electronic Design Automation, or EDA, tools) for universities, research institutes, and start-ups. A government-backed EDA platform would negotiate bulk licenses and host these tools for shared use.

  2025 action: Procure bulk EDA software licenses and establish an operational EDA Cloud platform by end-2025.

- Decision 4: Co-fund semiconductor training centers and labs. Jump-start infrastructure investment for talent development by co-investing in national semiconductor training and R&D hubs. Through public–private partnerships (PPPs), the government would match funding (e.g., 50–60%) for critical facilities, with industry contributing the remainder – along with operational expertise.

  2025 action: Commit funding in 2025 for at least three national semiconductor hubs, and kick-start two pilot projects (e.g., a training fab and an advanced packaging center) within the year.

- Decision 5: Establish a Semiconductor & Tech Talent Governing Body. Form a high-level talent governing body – comprising representatives from government, industry, and academia – to coordinate the national talent agenda, with the goal of aligning efforts and driving public–private partnerships.

  2025 action: Officially launch the governing body by 2025 to signal whole-of-government commitment.

Collectively, such moves would give a huge boost to Viet Nam's talent engine and send a powerful signal to investors – and to the country's talent – that the country "means business" in semiconductors.

An integrated roadmap to 2035: Objectives and proposals

Important as quick wins are, Viet Nam's semiconductor ambitions also require sustained effort through 2030 and beyond. This is best achieved through an integrated roadmap to 2035, aligned with the country's broader industry development timeline. The proposed roadmap is built on existing government commitments – such as the initial 2030 targets and the existing policy landscape – as a foundation.

Underlying these proposals are the following principles:

- ☑ Close today's gaps and pre-empt tomorrow's: Every action is chosen because it tackles current skills shortages while anticipating future gaps as Viet Nam climbs the value chain.
- ☑ Build a full talent pipeline - stock and flow: These measures strengthen the stock of existing scientists, engineers, and technicians, while enlarging the flow of pnew graduates and upskilled workers.
- ☑ Act on three margins of scarcity: Interventions boost the extensive margin (quantity of qualified talent), the intensive margin (depth of specialization, interdisciplinarity, frontier knowledge and skills), and the integrative margin (training-to-work, lab-to-fab, R&D-integrated training).
- ☑ Sequence "quick wins" with long-term gains: Early, visible results (e.g., bootcamps, shared EDA licenses) build momentum while laying foundations (e.g., cleanrooms, PhD pipelines) for the 2035 horizon.
- ☑ Augment, be adaptable, and scalable fora broader "Strategic Tech" agenda: The recommendations are semiconductor-centric today, but every instrument can later scale to support other strategic technologies.

Key proposals, summarized in Table ES-2, ensure that higher education institutions, research institutes, and industry can effectively collaborate and innovate. They address key opportunities and current gaps resulting in the talent challenges, including faculty shortages and retention challenges, underdeveloped postgraduate programs, teaching and research infrastructure shortfalls, fragmented industry-university engagements, low innovation and entrepreneurial outputs, and nascent AI integration in training programs and research.

Table ES-2. Four intervention pillars and key implementation elements

	INTERVENTION PROPOSALS	TIME HORIZON*
PILLAR 1: IGNITE TALENT		
1	Semiconductor Fellowship Program (postgraduate): i) MSc/PhD scholarships to study in leading institutions in Viet Nam or abroad; ii) mix of domestic and overseas "twinning" degrees; iii) bonding agreements to work in Viet Nam.	ST / MT
2	Advanced upskilling & professional conversion: i) 3-6-month bootcamps run by National Innovation Center, anchor universities, and firms; ii) vendor academies by leading firms; iii) Professional Conversion Program for mid-career engineers from adjacent sectors; iv) Multinational (MNC) firms-led on-the-job upskilling with strong government incentives.	ST
3	Faculty Excellence Fund / Program: i) fully-funded PhDs abroad for young lecturers with return grants; ii) visiting-professor & diaspora tracks; iii) performance incentives for research and curriculum upgrades; iv) sabbaticals in industry.	ST / MT
4	Semiconductor Faculty Fellowship (nucleus leaders): competitive grants to create specialized labs, covering equipment and PhD students.	MT/ LT
5	Industry experience – internship & apprenticeship: i) paid internship and apprenticeship in firms or labs with stipends subsidised by Investment Support Fund (potentially).	ST
6	Industry-linked curriculum reforms: i) joint Academic & Industry Advisory Boards update reference curricula annually; ii) embed Electronic Design Automation (EDA) tool certification, AI-hardware and supply-chain modules; iii) shared courses and training programs across leading universities.	ST
PILLAR 2 – BUILD SHARED R&D INFRASTRUCTURE		
7	National IC Design & Prototyping "Commons": central Electronics Design Automation (EDA) license library; High performance computer (HPC), IP core repository and Multi-project wafer (MPW) shuttle services hosted by national hubs/centers, open to universities and startups.	MT
8	University Lab Upgrade Program: competitive US$5-10 m grants to 5-10 universities to upgrade university training labs, including operation and maintenance budget and technician training.	ST
9	Pilot Advanced Packaging & Testing Facility: shared 2.5D/3D pilot line jointly funded and established in partnership with the industry; integration of workforce training and translational R&D; feasibility study completed by 2026.	MT
10	Public-Private Partnerships (PPPs) for large-scale infrastructure: full-scale national semiconductor and high tech hubs (for interlocked critical and emerging technologies), financed with 50:50 private-public split; 10-15 percent of capex reserved as maintenance endowment.	MT / LT
PILLAR 3 – CATALYSE UNIVERSITY–INDUSTRY–GOVERNMENT INNOVATION		
11	Matching-grant consortia for R&D: Semiconductor Innovation Challenge funds joint university–industry projects on a 50/50 cost share; pilot call 2025-26 with international expert panel.	ST
12	Technology-transfer offices, commercialisation funds & start-up vouchers: strengthen university Technology Transfer Office, provide proof-of-concept grants, and issue startup vouchers to spinoffs.	ST / MT

13	VITALS program & pilot-line innovation hubs: a full scale program co-fund linking universities with industry and local firms with MNCs for knowledge and technology spillovers; upskilling, expanding advanced packaging and pilot lines, and track spillover (Pillar II-9 and II-10).	MT / LT
PILLAR 4 - GOVERN & FINANCE FOR RESULTS		
14	Semiconductor and Tech Talent governing body: i) an apex steering body under the National Science, Technology, Innovation and Digital Transformation Steering Committee; includes ministries, universities and industry; ii) a coordinating agency for unified action plan, implementation, and progress tracking.	ST
15	One-stop financing platform: digital portal/platforms pooling multiple available funding sources; single call for integrated talent-and-innovation proposals; dynamic public private matching ratios.	ST

*Note: Time horizon is indicative of the implementation start of the proposal. Short term (ST) refers to approximately 1-2 years (2025-2026), medium term (MT) 3-5 years (2027-2030), long term (LT) beyond 5 years (2031-2035), from 2025.

Risks & mitigation

No ambitious program is risk-free. Viet Nam s semiconductor talent initiative faces four main risks, all of which can be mitigated with sufficient foresight:

Risk 1: Brain drain: After advanced training (especially abroad), some individuals may choose to leave Viet Nam for higher-paying opportunities, undercutting the local talent pool.

Mitigations: Implement bonding agreements for scholarship recipients. Simultaneously, improve local incentives to return by creating attractive R&D roles and career pathways in Viet Nam. Also, engage overseas Vietnamese experts in domestic projects, creating a "brain circulation".

Risk 2: Fiscal stress: The program' s sizable public funding (about $2 billion over 2026–2030) could face shortfalls if economic conditions change or government priorities shift.

Mitigations: Prioritize the initiative as a national priority with multi-year budget earmarks to protect and sustain funding. Phase the project into scalable segments to ensure core elements (scholarships, critical labs) are funded first if budgets tighten. Embed private co-financing and pursue alternative funding sources (e.g., industry contributions, donor support). Demonstrate early successes to sustain political support.

Risk 3: Demand volatility: A global downturn could see chip demand fall or a new disruptive technology could temporarily alter labor demands.

Mitigations: Design curricula and training with flexibility and breadth. Emphasize fundamental skills (e.g., solid electronics engineering, programming, problem-solving) that transcend industry cycles. Future proof talent programs through continuous updates. Avoid narrow over-specialization, maintain an agile training and workforce development system and a culture of life long learning.

Risk 4: Private-sector participation: Private-sector actors may fail to co-invest or engage to the extent expected, due to lack of awareness, mistrust, or their own constraints.

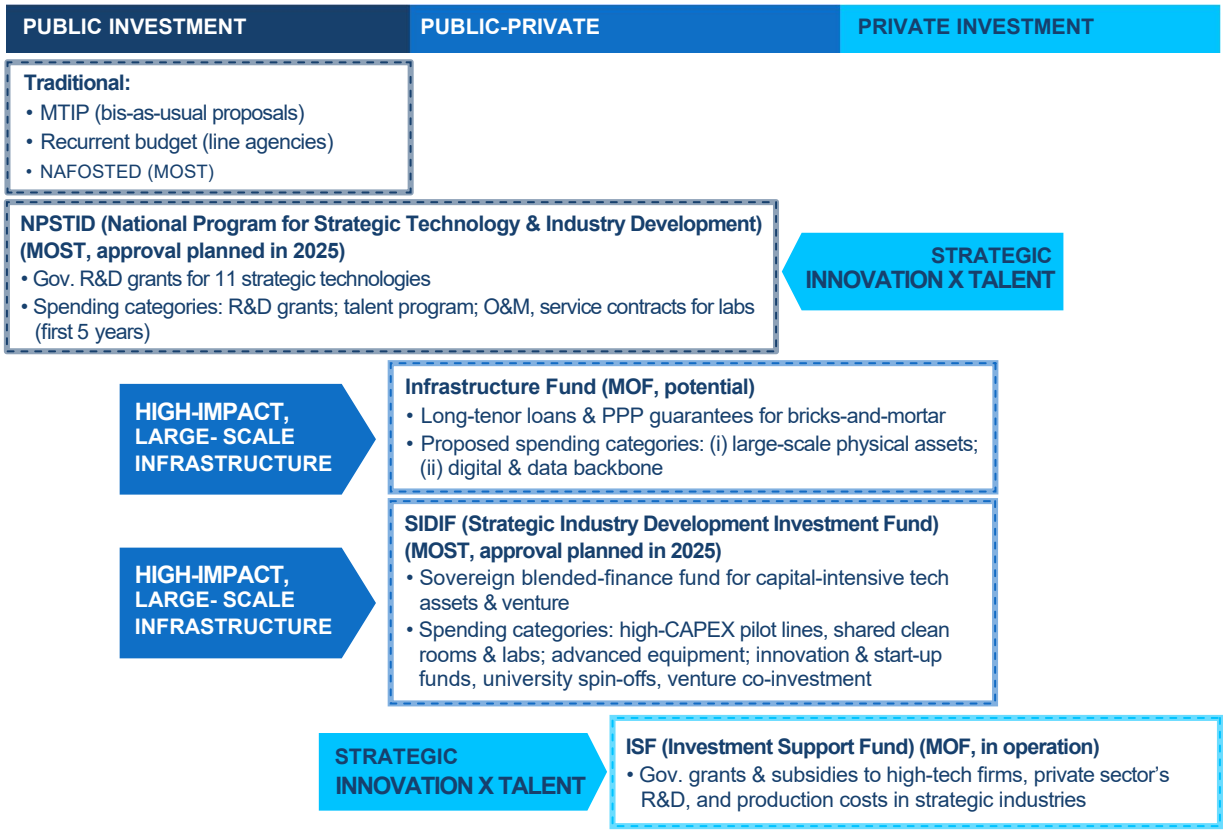
Mitigations: Socialize the program and its incentives through the Talent Council and industry associations. Simplify processes for firms to engage (e.g., easy applications for matching grants). Highlight quick wins to build momentum.

Jobs upside vs fiscal cost

Manageable expenditure: Investing in semiconductor talent will require substantial funding, but the growth dividend it will yield far outweighs the cost. The total program is estimated to need about $2 billion over 2026–2030 (combined public and private investment). This is roughly 0.1–0.2% of Viet Nam's GDP per year – a manageable sum considering the strategic importance of semiconductors and the expected returns. With public debt relatively low, Viet Nam has the fiscal space to act now.

Return on investment: In return for this investment, Viet Nam stands to gain a vibrant high-tech industry generating thousands of well-paid jobs, greater domestic value-add (reducing reliance on imported high-tech inputs), and economy-wide productivity gains from technology diffusion. Budget outlays on scholarships, faculty, and labs should primarily be viewed as investment in future growth, not mere expenditures.

Figure ES-5. Aligning public and private resources for semiconductors and tech talent



Bottom line

Semiconductor and tech talent is the make-or-break factor for Viet Nam's high-tech ambitions. Unlike low-cost labor in apparel or assembly – where Viet Nam has excelled – the semiconductor industry demands deep skills and continuous innovation. Against this once-in-a-generation landscape of opportunities, a lingering question sometimes arises: could Viet Nam produce "too many" STEM graduates, too quickly? Global evidence – and Viet Nam's own experience – suggests the opposite – a greater risk is having too few. At every juncture when Viet Nam has raised its high-tech ambitions, the real bottleneck has been a shortage of engineers and scientists – never an excess.

PART I.

THE CASE FOR ACTION: INVESTING IN THE BRAIN OF THE "BRAINS"

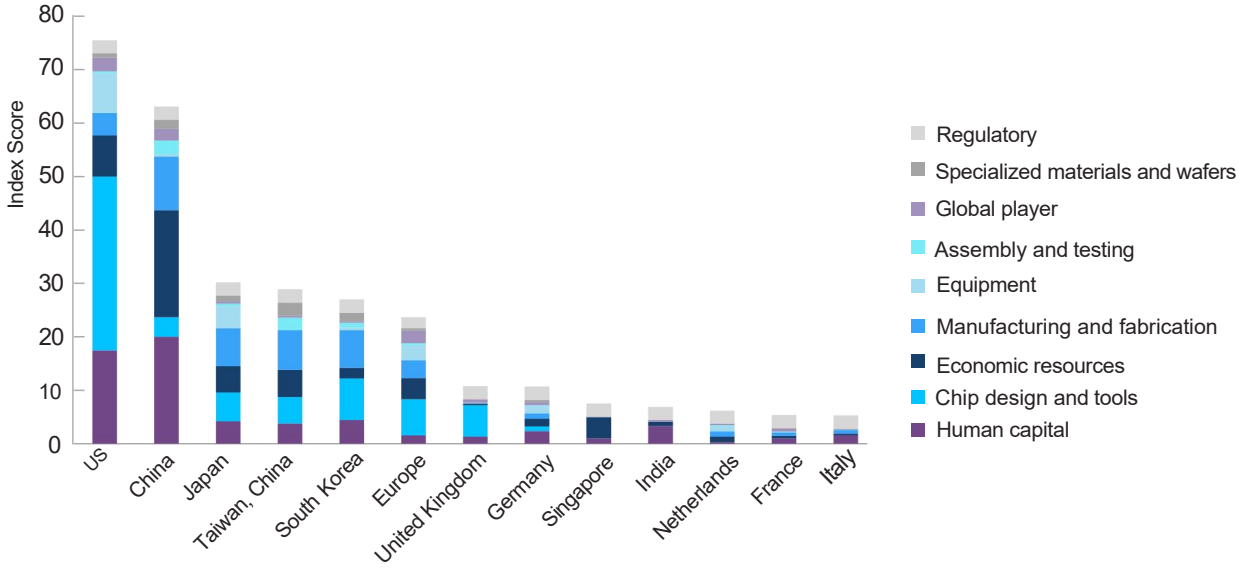
1. VIET NAM' S SEMICONDUCTOR MOMENT: MOVING UP THE VALUE LADDER

1.1. Semiconductors, AI, technology convergence, and the tech talent race

The world is entering an artificial intelligence (AI)-driven semiconductor supercycle, with unprecedented demand for chips powering everything from generative AI to electric vehicles (EVs). Global semiconductor sales are projected to double this decade – surpassing US$1 trillion by 2030 – fueled largely by AI, data centers, EVs, and Internet of Things (IoT) adoption.[01] The rise of generative AI models in 2023, for example, triggered a rush for advanced AI accelerators (graphics processing units – GPUs), causing supply bottlenecks and soaring prices. This AI supercycle could generate an estimated US$15 trillion in economic output and 100 million jobs by 2030 across all sectors – if the tech infrastructure can keep up. National strength in domains like AI and semiconductors hinges on superior innovation ecosystems, human capital, and economic resources (Rosenbach et al., 2025).

AI and semiconductors are at the very core of global technological convergence. Technology convergence is accelerating across the tech stack of five of the most critical and emerging technologies – AI, semiconductors, biotech, space, and quantum – in which advancements in one technology create network effects that spur progress in others, often in unpredictable ways (Park, 2019; Rosenbach et al., 2025; Anil, 2025). Powerful AI models are already accelerating chip design and drug discovery, while advances in quantum research are opening new frontiers in semiconductor materials, particularly for next-generation and quantum computing applications.

Figure 1. Semiconductor technology index by economies and foundational pillars



Source: The Harvard' s Belfer Center Critical and Emerging Technologies Index, Defense, Emerging Technology, and Strategy (DETS) Program (accessed on June 22, 2025).

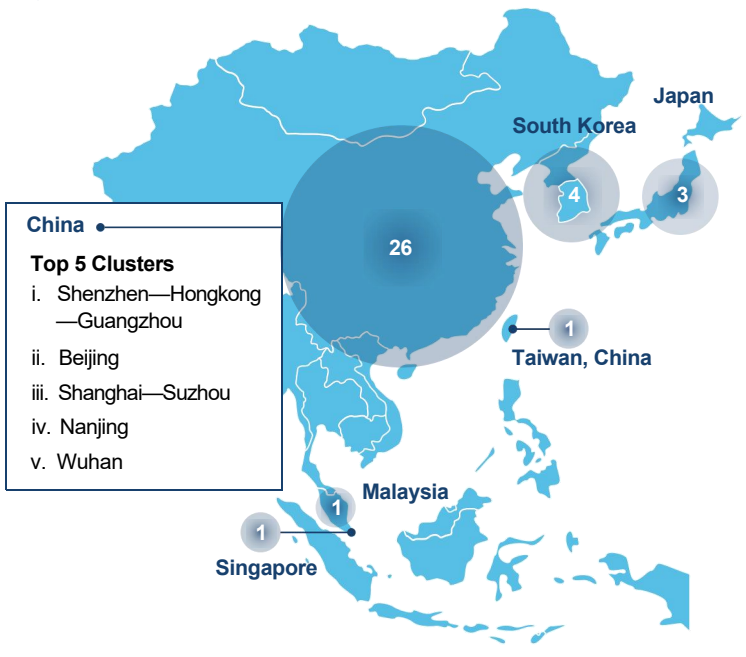
Note: The index is calculated by assigning different weights to key dimensions (or pillars) based on their relative importance. Three top pillars for semiconductors technology are: (i) Chip design and tools (weighted at 32.5%) captures a nation' s ability to architect and define next-generation chips; (ii) Human capital (weighted at 30%) captures the depth and quality of a nation' s semiconductor talent pool; (iii) Economic resources (weighted 20%) captures the financial resources of a nation available to its semiconductor ecosystem.

01 Burkacky, O., Dragon, J., & Lehmann, N. (2022, April 1). The semiconductor decade: A trillion-dollar industry. McKinsey & Company. Retrieved from https://www.mckinsey.com/industries/semiconductors/our-insights/the-semiconductor-decade-a-trillion-dollar-industry

Semiconductors are the "brains" behind all modern technologies—from AI and digital transformation to frontier breakthroughs—while talent is the "brain" behind the chip itself. The bedrock of semiconductors, as a critical technology and industry ecosystem, is founded on technology (chip design and tools), human capital (specialized workforce and science, research and development (R&D) talent), and capital (economic resources) (Rosenbach et al., 2025; BCG, 2022; SIA & BCG, 2020; SIA & BCG, 2021). Five East Asia economies China, South Korea, Japan, Singapore, and Taiwan (China) rank atthe global top for both AI and semiconductor technologies (Figure 1). Massive science, technology, engineering, and mathematics (STEM) graduate outputs, deep engineering talent pools, and robust researcher pipelines power these strong East Asian innovation ecosystems. For example, Singapore s semiconductor strategy leans on its highly skilled workforce, the talent-innovation flywheel, modern infrastructure, and strong ecosystem linkages, to move from electronics manufacturing into chip design and advanced packaging.

The East Asian economies in the global top 10 positions for semiconductors technology also host 36 of the global top 100 science and tech (S&T) clusters according to the Global Innovation Index 2024.[02] All the world' s five biggest S&T clusters are now located in East Asia, and in the top 100 there are 26 clusters in China, four in South Korea, three in Japan, and one each in Malaysia, Taiwan (China), and Singapore (Figure 2, Table 1). One common feature of these S&T clusters is that they always coalesce around flagship research universities with the latter acting as the anchor for talent, basic research, and spin-off activity (See more in Annex 2). For example, inChina s two biggest hubs Shenzhen Hong Kong Guangzhou and Beijing Shenzhen University, the Hong Kong universities, and SUSTech in the Pearl River Delta, together with Tsinghua and Peking University in the capital, supply the bulk of the region' s graduate engineers and host joint labs with firms such as Huawei, CATL, and SMIC. South Korea s four WIPO-listed clusters are likewise university-centered with Seoul Incheon around Seoul National University and the "Techno Valley" of Yonsei and Korea University.

Figure 2. East Asia: Global top 100 Science and Tech clusters



The boundaries, colors, denominations and other information shown on any map in this work do not imply anyjudgement on the part of The World Bank concerning the legal status of any territory or the endorsement or acceptance of such boundaries.

Table 1. Global ranking of S&T clusters

Number of S&T clusters in the global top 100 in 2024				
	Top 10	Top 20	Top 50	Top 100
US	3	6	11	20
China	4	8	15	26
Taiwan, China	0	0	1	1
South Korea	1	2	2	4
Japan	2	3	3	3
Singapore	0	0	1	1
Malaysia	0	0	0	1

Source for Figure 2 and Table 1: WIPO – Global rankings of science and technology clusters, 2024.

Note: Clusters are defined as geographical areas that show a high density of inventors and scientific authors. Two innovation metrics are used to construct the top 100 S&T clusters worldwide are location of inventors listed on published patent applications and authors listed on published scientific articles.

02 WIPO (2024). Global Innovation Index 2024: Science and Technology Cluster Ranking. Retrieved at https://www.wipo.int/en/web/global-innovation-index/2024/science-technology-clusters

Table 2. Overview of government's financing commitment, engineering or STEM graduates, current workforce in semiconductors

Country	Government's committed budget (selected, not exhaustive information)			Annual engineering/ STEM university graduates	Semiconductor current workforce
	Industry/ ecosystem	R&D & innovation	Workforce development		
Viet Nam[03]			US$1.08 bil. for semiconductor (2025-2030) (not yet appropriated)	148,000 (2023)	Approximately 15,000 – 17,000 (2025) (See Annex 3)
China[04]	>US$50 bil. via China IC Industry Investment Fund (since 2014)			1.9 mil. (2022), including 170,000 in microelectronics (2022)	570,000 (2022)
Singapore[05]		US$18.8 bil. for R&D (2021-2025) via RIE2025 (4 microelectronics pillars); US$748 mil. for biotech & semiconductor R&D infrastructure	US$75 mil. for internships & traineeships	7,000 university STEM graduates; 2,500 polytechnic diplomas (2022)	35,000 (2023)
South Korea[06]	US$246 bn for the Yongin Semiconductor Mega-Cluster (2023-2042). Project covers six advanced fabs plus 200+ supplier & fabless firms; designated a national strategic complex in 2024.		US$1.2 bil. for K-Semiconductor Strategy 2021-2030	130,000 (2020)	180,000 (2021)
Malaysia[07]			US$5 bil. for 60,000 semiconductor engineers	50,000 (2018) with 10,000 engineers; 15,000 technicians	105,000 (2019)
Taiwan, China[08]		US$10 bil. (2024-2033) – Taiwan Chip-based Industrial Innovation Program		55,000 annual engineering graduates (2019-2022)	290,000 (2022)
India[09]	US$10 bil. via Semicon India Program in 2022		US$ 60 mil. for upskilling in 10 key technologies via FutureSkills Prime	2.5 mil. (2020); with 850,000 engineering grads (2019)	220,000 including adjacent industries

03 https://vir.com.vn/vietnam-commits-108-billion-to-train-50000-semiconductor-engineers-by-2030-110660.html; MOET of Viet Nam (2024).

04 CSIA White Paper 2023 – China "Big Fund" & IC Talent Plan; 2022 STEM Graduation Report – Ministry of Education

05 Ministry of Finance of Singapore 2025 Budget Statement; EDB Singapore – EITM Progress Report – Economic Development Board, 2023; MOE Singapore Graduate Diplomas 2022 – Ministry of Education; MOM Report on Semiconductor Workforce 2022 – Ministry of Manpower, Singapore

06 KSIA 2022 Annual Report – Korea Semiconductor Industry Association, 2022; SEMI Global Up/Reskilling Program Statistics – SEMI, 2023; KSIA 2031 Workforce Projection – KSIA, 2022

07 Malaysia TalentCorp & PSDC Report – Malaysian GOV, 2021–25; Dept. of Statistics Malaysia STEM Grad Data – Malaysian Government, 2018; "Malaysia semiconductor engineer shortage" – Malay Mail, Dec 2023

08 Executive Yuan Press Release on CBI Program; Taiwan Ministry of Education Graduate Statistics – MOE Taiwan, 2022; Taipei Times: Chip Industry Labor Gaps – Taipei Times & Executive Yuan, 2023

09 Higher Education in Science and Engineering – National Science Foundation (2023); IESA 2022 Semiconductor Workforce Report – Indian Electronics & Semiconductor Assoc., 2022; AISHE 2019 – India Engineering Graduate Numbers – Ministry of Education; https://www.pib.gov.in/PressReleasePage.aspx?PRID=1808676; https://government.economictimes.indiatimes.com/news/policy/futureskills-prime-meity-nasscom-industrys-joint-initiative-aims-to-create-up-skilling-re-skilling-ecosystem-in-10-emerging-technologies/87383517;

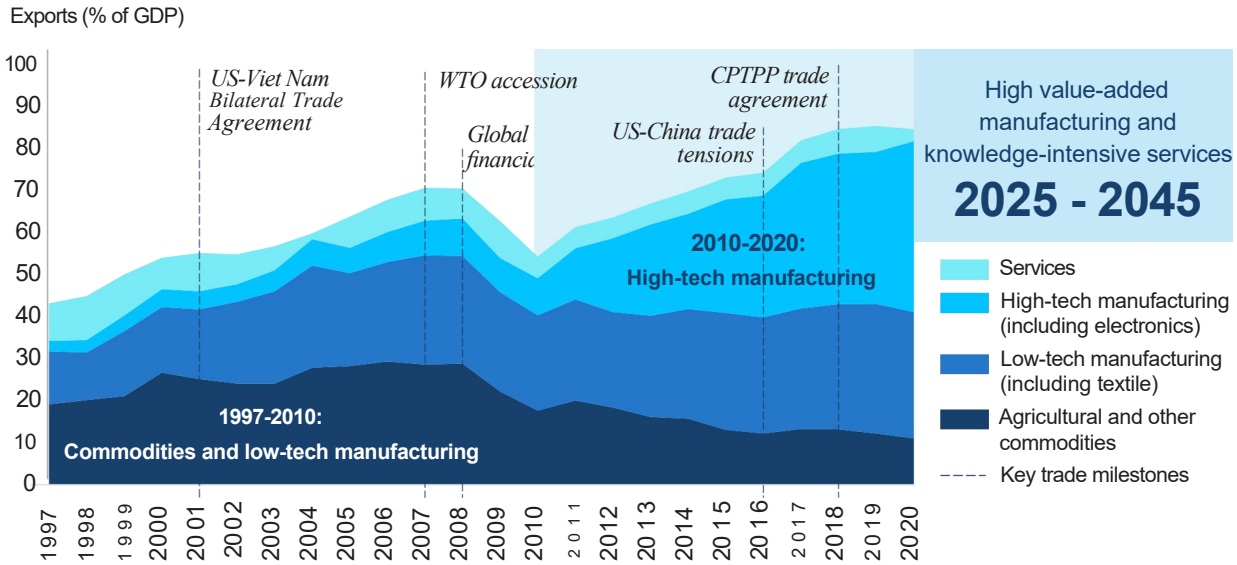
The unprecedented demand for chips has resulted in surging talent demand which has outpaced talent supply and led to a global chip talent crunch. Even with new incentives, the United States (US) projects its chip workforce will fall 67,000 short of demand by 2030 (SIA & Oxford Economics, 2023). China faces an immediate shortfall of around 200,000 chip engineers as of 2023 (CCIID & CSIA, 2023), South Korea anticipates a 54,000-worker gap by 2031, and Japan and others also report persistent talent deficits. Industry growth targets with the global sector aiming for US$1 trillion in revenue by 2030 are thus at risk due to talent scarcity. Table 2 presents a snapshot of government's financing commitments, workforce needs, and available pools in different economies, showing the need for immediate actions to ease the talent gaps.

More than a critical technology, the semiconductor industry straddles multiple pillars of the growth development agenda for a country like Viet Nam – demanding advanced skills and knowledge, driving innovation, and accelerating the infusion of digital technologies across industries. Semiconductors are the "brains" in all modern technologies (AI, digital transformation, other technological advancements), while talent is the brain behind the chips. It is simultaneously the most knowledge-, technology-, and capital-intensive industry. Success in this industry will not only mark progress in high-tech manufacturing but also help propel the country's broader transformation toward a knowledge-based, innovation-driven economy.

1.2. Viet Nam's semiconductor industry: the starting point

To achieve its 2045 high-income ambition, Viet Nam must again transform its economic model - this time by capturing higher-value activities like high-value, R&D-intensive services and advanced manufacturing (World Bank, 2024a). Viet Nam's economic structure has already shifted from commodities and low-tech manufacturing in the 2000s to high-tech electronics manufacturing in the 2010s. Its next chapter – envisioned for 2025–2045 – centers on high-value manufacturing and knowledge-intensive services and will hinge on leveraging innovation and a skilled, innovative workforce to climb further up the value ladder (Figure 3).

Figure 3. An evolving export growth model to reach Viet Nam's 2045 ambitions

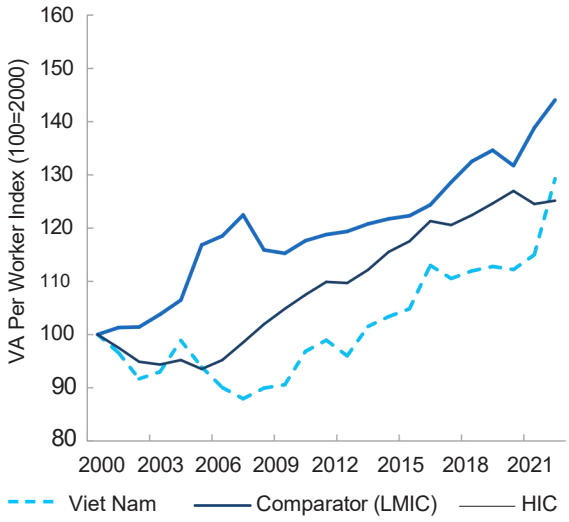


Source: World Bank (2024a).

Viet Nam's rising productivity in knowledge-intensive, innovation-oriented services is a promising sign for this transition. Over the past two decades, value-added per worker in knowledge-intensive service sectors has grown more rapidly in Viet Nam than in its lower middle-income peers, and it is now converging toward high-income economy levels (Figure 4). This outperformance signals Viet Nam's potential to leapfrog in certain knowledge industries.

For high-tech manufacturing, in the past decade, Viet Nam's electronics exports have skyrocketed - surpassing US$132 billion in 2023 - making the country one of the world's top electronics exporters. This track record signals a strong manufacturing base, yet it masks the fact that most of these exports come from assembly by foreign direct investment (FDI) firms, with limited local semiconductor value-add. Even so, Viet Nam's growing stature as a reliable, neutral manufacturing hub gives it a competitive edge in the current global market. Few countries at a similar stage of development combine Viet Nam's scale, stability, and cost competitiveness – factors that position it uniquely to attract semiconductor investment as the industry diversifies its supply chain.

Figure 4. Innovation services productivity



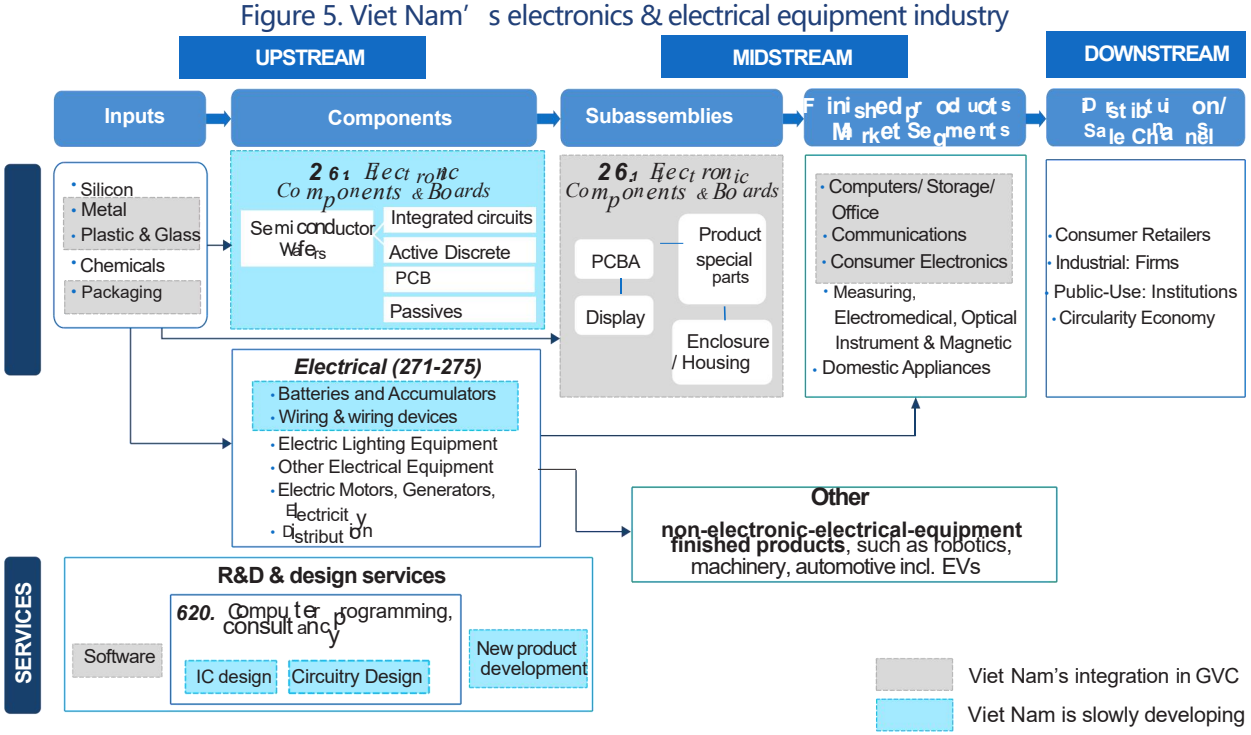
Source: World Bank staff compilation based on Country Growth and Jobs Dashboard (2025).

Note: HIC for high-income countries, LMIC for lower-middle-income countries, VA for value added.

Despite the promising outlook, Viet Nam's current role in the high-tech industries and services remains limited and concentrates on low value-added segments. Take the electronics and electrical equipment (E&E) value chain for example, the country participates mainly in lower-value segments – chiefly assembly, packaging, and testing (the "back-end" of chip production) – and a small amount of chip back-end design services (Figure 5). In practice, this means that while Viet Nam hosts large electronics manufacturing operations (e.g., Samsung plants), the sophisticated chip design and wafer fabrication steps are mostly done abroad. For instance, up to 85 percent of Viet Nam's electronics exports (as of 2024) are from foreign-invested firms, primarily assembling components designed elsewhere (GSO, 2025). Domestic firms and workforce are concentrated in basic midstream tasks, with minimal presence in upstream R&D or downstream high-tech fabrication. For semiconductors, Viet Nam has yet to capture significant domestic value-add – most high-value work (intellectual property (IP) design, advanced process engineering) is currently done outside the country.

The semiconductor multipliers: success in the semiconductor industry has a significant multiplier effect on Viet Nam's broader economy. Crucially, semiconductors manufacturing is part of the broader E&E value chain – a sector in which Viet Nam has firmly established itself as a key player over the past 15 years – while chip design is part of the growing computer programming services. A local semiconductor ecosystem supports electronics, AI, telecommunications, and other industries that rely on chips. It also creates high-paying jobs and knowledge spillovers (through supplier networks, startups, etc.). Moreover, semiconductors align with Viet Nam's digital transformation and security goals – having domestic capability in chips is increasingly seen as a strategic asset. Third, regional examples show that it is possible: Taiwan (China), South Korea – even Malaysia – have grown from assembling chips to designing and innovating them by systematically investing in workforce development and building R&D capacity.

Figure 5. Viet Nam's electronics & electrical equipment industry



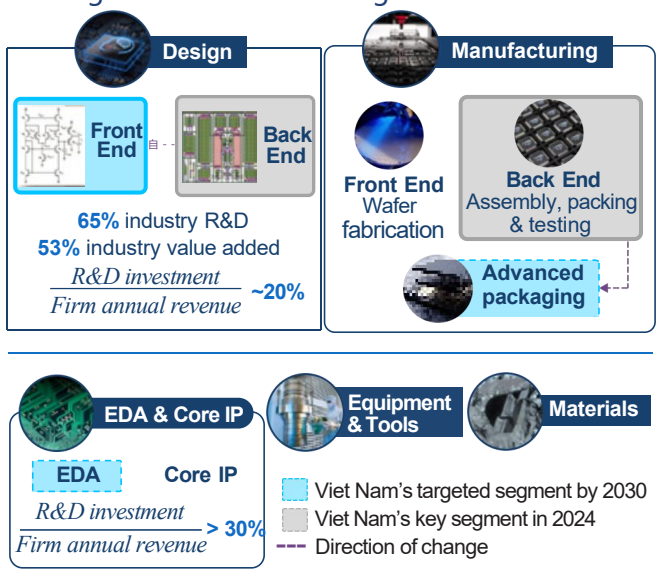
Source: World Bank staff elaborated based on International Finance Corporation (unpublished, 2020).

Note: GVC for global value chain. PCB for printed circuit board. PCBA for printed circuit board assembly.

1.3. Three windows for Viet Nam in upgrading the semiconductor value chain

Viet Nam has the potential to move up the semiconductor value chain through a progression of increasingly complex segments: consolidating standard Assembly, Testing & Packaging (ATP) and back-end Integrated Circuit (IC) design, advancing into Advanced Packaging, and scaling up IC design, including moving up front-end IC design capabilities (Figure 6). Each stage offers distinct opportunities for Viet Nam to capture greater value and create skilled jobs, provided that supporting policies and workforce development keep pace with industry needs. The industry assessment (Nguyen, Tran, and Bergman, 2025), which included in-depth interviews with Viet Nam's leading semiconductor firms, such as Intel, Marvell, and Faraday, has identified the following potential windows for Viet Nam in upgrading the semiconductor value chain.

Figure 6. Semiconductor global value chain



Assembly, Testing & Packaging: leveraging a strong foundation

The presence and scale of these global players underscore Viet Nam' s rising stature in back-end manufacturing. Basic ATP is the traditional entry point of many countries into semiconductor manufacturing, and Viet Nam has firmly established itself in this segment. Viet Nam has attracted substantial investments from top global semiconductor manufacturers.

- Intel Intel s Ho Chi Minh City plant is Intel s globally largest assembly and test site, with about 6,000 employees, and has produced over 3.9 billion units and contributed more than US$96 billion in export value since its opening in 2010 and plans further expansion and tech upgrades.[10] Intel s Viet Nam operation alone accounts for over 60 percent of the company s global output in assembly and testing.
- Amkor Technology In 2023, Amkor Technology opened a new US$1.6 billion "smart factory" in Bac Ninh a state-of-the-art factory for advanced system in package (SiP) and memory packaging for consumer and telecom applications which is slated to become Amkor s largest operation worldwide (Amkor, 2023).[11]
- Hana Micron – A leading South Korean outsourced semiconductor assembly and test (OSAT) firm, Hana Micron is expanding in Bac Giang with ambitions to make Viet Nam its biggest production hub.[12] Its Viet Nam operations focus on IC assembly for mobile devices and are actively developing advanced packaging techniques, expecting substantial revenue growth.

Equally important, they bring know-how and supplier networks that can benefit local industry and Viet Nam' s key strengths in ATP provide a solid platform for upgrading along the value ladder:

- Established OSATbase A well-developed packaging and testing industry already exists. Market leaders like Intel and Amkor have proven capabilities that could be transferred to Viet Nam s operations when conditions allow, accelerating the move into more advanced packaging. This existing base instills confidence that Viet Nam can handle greater scale and complexity in chip packaging.
- Skilled labor and wage advantages – Viet Nam offers a young, trained workforce at competitive cost, e.g., experienced semiconductor engineers earn roughly 50 percent of Japan s and barely 1/8 of U.S. salaries. This ample talent supply is ideal for ATP activities and is steadily growing with graduates from technical universities and vocational programs.
- Government support The government actively promotes semiconductor investment through tax incentives, subsidies, and streamlined regulations. Policies include corporate tax breaks for high-tech firms and funding for workforce upskilling and retraining, e.g., through the government-funded Investment Support Fund (ISF) established in 2024.

Leveraging these strengths, Viet Nam can continue to solidify its ATP segment - attracting new factories and expanding existing ones. While basic assembly and test are relatively lower in the value chain, they generate massive employment and establish Viet Nam as a reliable manufacturing partner. Just as critically, a strong ATP base serves as the springboard to higher-value activities. Experience gained in managing quality control, logistics, and tech transfers in ATP builds essential industrial know-how, laying the foundation required to venture into more complex processes like advanced packaging.

10 Intel. (2022). Intel taps factory network to overcome substrate shortages. Retrieved from https://download.intel.com/newsroom/archive/2025/en-us-2022-05-26-intel-taps-factory-network-to-overcome-substrate-shortages.pdf

11 Amkor. (2023). Amkor inaugurates latest factory in Vietnam. Retrieved from https://amkor.com/blog/amkor-inaugurates-latest-factory-in-vietnam/

12 Government of Vietnam. (2023). South Korea's Hana Micronto invest US$1bn in Viet Nam chip production. Retrieved from https://en.baochinhphu.vn/south-koreas-hana-micron-to-invest-us1bn-in-viet-nam-chip-production-111231005100656848.htm

Advanced Packaging: a new strategic segment

Advanced packaging is Viet Nam's chance to leapfrog within the manufacturing domain - moving from primarily labor-intensive assembly to more technology-intensive production. This new segment is transforming the value chain, making the traditionally low-profile packaging stage into a critical, R&D-intensive part of chip production. Unlike traditional packaging, advanced packaging involves techniques such as 2.5D/3D chip packaging, chiplet integration, and fan-out wafer-level packaging, which directly improve chip performance and density, thermal management, and energy efficiency (SIA & BCG, 2021).[13]

With advanced packaging, package design and manufacturing now require closer collaboration between chip designers, foundries, OSATs, and materials suppliers than ever before. The global market for advanced packaging, roughly US$48 billion, is about 8 percent of the entire semiconductor market today and is forecast to double by 2030, growing faster than the overall semiconductor industry. This surge is fueled by exploding demand for AI accelerators and high-performance chips that cannot be realized by silicon scaling alone instead, they rely on combining multiple chips (chiplets) in one package and vertically stacking dies, which advanced packaging techniques offer.

Viet Nam has an opening to position itself as a regional leader in advanced packaging, building on its ATP success. Notably, Intel Viet Nam houses significant R&D activities, including advanced 3D packaging technology (Foveros), and Amkor Viet Nam offers turnkey solutions from design to electrical testing, focusing initially on Advanced SiP and memory production for global export.[14] The presence of such advanced processes on Vietnamese soil is an excellent start. To truly capitalize on this trend, Viet Nam will need to scale up the required skills, infrastructure, and ecosystem:

- Skilled workforce development: Advanced packaging is multidisciplinary and requires more specialized (advanced) engineering and research skills (e.g., in package design, thermal management, materials science) which are currently in short supply in Viet Nam. These skills gaps are further elaborated in the next sections.
- Infrastructure, technology, and equipment access: Many advanced packaging steps (like 3Ddie bonding, wafer-level assembly) demand expensive, cutting-edge equipment, cleanroom facilities, and processes that Vietnamese firms have limited access to. Technology transfer from global OSAT leaders and investing in shared facilities (e.g., an advanced packaging R&D center or pilot line, as discussed in Part II) are critical to support domestic industry climb the learning curve.
- Targeted investment incentives: Given the dual R&D and capital-intensive nature of this segment, government incentives are critical specifically for advanced packaging investors. That includes deploying grants and R&D support for this niche and offsetting the costs of cleanroom construction, equipment, or workforce training for companies.

Addressing these needs, Viet Nam can attract a new wave of advanced packaging projects and ensure existing ATP investors upgrade their local operations. The payoff would be significant: advanced packaging would not only raise Viet Nam s value-add per chip, but also create upstream and downstream linkages (in design, materials, and subsystem integration) that deepen the local industry. Moreover, mastering advanced packaging aligns Viet Nam with the latest industry shift toward chiplet architectures and 3D integration, securing its place in emerging supply chains for AI and high-performance computing chips.

---

13 BCG. (2024). Advanced packaging is reshaping the chip industry. Retrieved from https://www.bcg.com/publications/2024/advanced-packaging-is-reshaping-the-chip-industry

14 Intel. (2024). Get to know Intel sites: Vietnam. Retrieved from https://community.intel.com/t5/Blogs/Intel/We-Are-Intel/Get-to-Know-Intel-Sites-Vietnam/post/1654126; Amkor. (n.d.). Amkor Technology Vietnam. Retrieved from https://amkor.com/amkor-technology-vietnam/

IC Design: capturing high-value innovation

Expanding Viet Nam's IC design capabilities is critical for the country to capture high value and foster a homegrown semiconductor ecosystem. Atthe top end of the value chain, IC design represents the most knowledge-intensive segment and the locus of innovation (chip architecture, logic design, IP creation). Encouragingly, Viet Nam's IC design sector has been gaining traction over the past decade. It is now home to around 40 design companies employing over 5,600 engineers, a talent pool that is projected to double in the next five years.

The mix of international and local firms signals a maturing ecosystem with growing expertise and diversification into areas like AI, wireless communications, and consumer electronics design. A few globally leading firms are operating in Viet Nam: Renesas (Japan) designs microcontrollers and System on Chip (SoC) in Ho Chi Minh City (HCMC), Qualcomm develops mobile chipsets in Hanoi and HCMC, and Marvell is making Viet Nam its third-largest design base globally after the US and India. Meanwhile, Synopsys and Cadence, leading electronic design automation (EDA) tool providers, have set up offices and training partnerships. There are also growing home-grown firms, such as FPT Semiconductor, TMA Solutions, and Viettel High Tech, as well as Vietnamese-founded companies with global headquarters and main operation sites in Viet Nam like Savarti, Uniquify, and Inphi Corp., designing specialized chips for power management and IoT.

Viet Nam brings several competitive advantages to IC design that underpin these opportunities.

- Cost-competitive engineers: An experienced Vietnamese chip design engineer earns roughly half the salary of a counterpart in Japan and only a fraction of a Silicon Valley salary.
- Government support and incentives: High-tech enterprises in IC design are eligible for tax breaks and reduced corporate income tax rates, and specific R&D projects can receive state grants.
- Accelerating knowledge transfer: Through on-the-job training and mentorship, local designers are acquiring know-how in modern chip design methodologies.

These strengths give Viet Nam a foothold in IC design, but the ambition is to move from doing primarily back-end design services toward front-end design of building IP and SoCs products. Global market trends are opening niches that Viet Nam-based teams can exploit. For example, the demand for specialized and application-specific integrated circuits (ASICs) is surging as companies seek custom solutions for AI, edge computing, 5G, and other domains. This is expanding the pie of design work worldwide, and Viet Nam can capture slices of it by focusing on areas that match its growing expertise, for example, designing AI-oriented microcontrollers, power management ICs, or chips for medical devices – all identified as promising avenues in Viet Nam's assessment.

With the right talent pipeline, Viet Nam's design sector can grow in both scale and scope, creating higher-paying engineering jobs and indigenous innovation capacity. Over time, a robust IC design segment will also synergize with advanced packaging and manufacturing – local designers working hand-in-hand with packaging engineers can co-optimize chip-package systems, an approach now vital for improving performance and cost (as seen in Design Technology Co-Optimization practices at leading firms). In essence, investing in IC design capabilities today not only yields direct economic benefits but also anchors Viet Nam more firmly in the innovation-driven layers of the semiconductor value chain.

In addition, to bolster Viet Nam's semiconductor industry, a strengthened IP framework is essential. This requires refining patent laws to specifically address semiconductor innovations and processes, ensuring robust protection across all relevant IP categories – including patents, trade secrets, copyright, and Semiconductor Chip Protection (Mask Work Rights or Layout Designs). Furthermore, enacting comprehensive trade secret

legislation to safeguard critical technical information, clearly defining copyright for software and design tools, enhancing enforcement through specialized courts and customs controls, increasing public awareness of IP rights, and aligning national IP laws with international standards are crucial steps. Addressing these key areas will cultivate a more secure and appealing landscape for both domestic ingenuity and foreign investment within Viet Nam's semiconductor sector.

1.4. Bottom line: balance a fine line between solidification and moving up

Developing these opportunities requires a balance between broad-based growth and niche innovation (Table 3). Viet Nam needs to continue consolidating its ATP base, which generates wide employment for a diverse workforce, while also pursuing R&D-intensive niches like advanced packaging and chip design. The ATP segment can create thousands of jobs across varying skill levels, anchoring an inclusive semiconductor workforce. In contrast, moving into design and advanced packaging demands deeper expertise and highly specialized teams, yielding smaller labor pools. Balancing this breadth and depth is crucial: a strong ATP foundation provides stability and scale, as higher-value segments build Viet Nam's innovation capacity.

The stage is thus set – Viet Nam has the intent and initial tools to become a player in semiconductors. Building on more recent, groundbreaking changes in the prioritization of the science-technology-innovation-digital development, quality workforce, and private sector development agenda, to truly seize the moment, Viet Nam needs an integrated push – aligning government, universities, industry, and investment around the semiconductor opportunity. The next sections, based on the identified opportunities for Viet Nam in the global value chain, discuss where and how talent is the binding constraint and the nature of Viet Nam's skills gap in this field, including a deeper look at the constraints on the supply side, especially, the higher education system.

Table 3. Viet Nam's semiconductor industry: Opportunities and challenges

Core Activity	Comparative Advantage / Opportunity	Talent & Implementation Challenges
ATP – Strengthen foundation	• Established OSAT base with major investors (Intel, Amkor, etc.) • Cost-competitive manufacturing hub and supportive government strategy • Global supply-chain shifts creating demand for diversified ATP locations	• Need to train and scale a large technician/ engineer workforce • Gaps in experienced managers and specialists • Must improve local supplier linkages and infrastructure to support high-volume production
Advanced Packaging – Next-gen backend tech	• Leverage existing ATP foothold to attract 2.5D/3D packaging projects • Rising regional demand for chiplet integration and SiP solutions • Early mover advantage with new advanced packaging facilities already in Viet Nam	• Shortage of specialized packaging engineers and R&D personnel • High capital requirements and technical know-how for new processes • Requires industry–academia partnerships to build skills in materials, thermal, and design integration
IC Design – From back-end to front-end	• Large pool of STEM graduates and information technology (IT) talent to tap into IC design training • Increasing interest from global fabless and design firms in Viet Nam as a cost-effective design center • Government push (scholarships, EDA tool support) and diaspora talent can jump-start design capability	• Limited supply of experienced chip designers and architects • Education system and curricula needing updates for semiconductor design • Smaller, highly specialized labor pool (often requiring MSc/PhD) and risk of brain-drain without local R&D growth

2. TALENT IS SIMULTANEOUSLY THE DRIVING FORCE AND BINDING CONSTRAINT

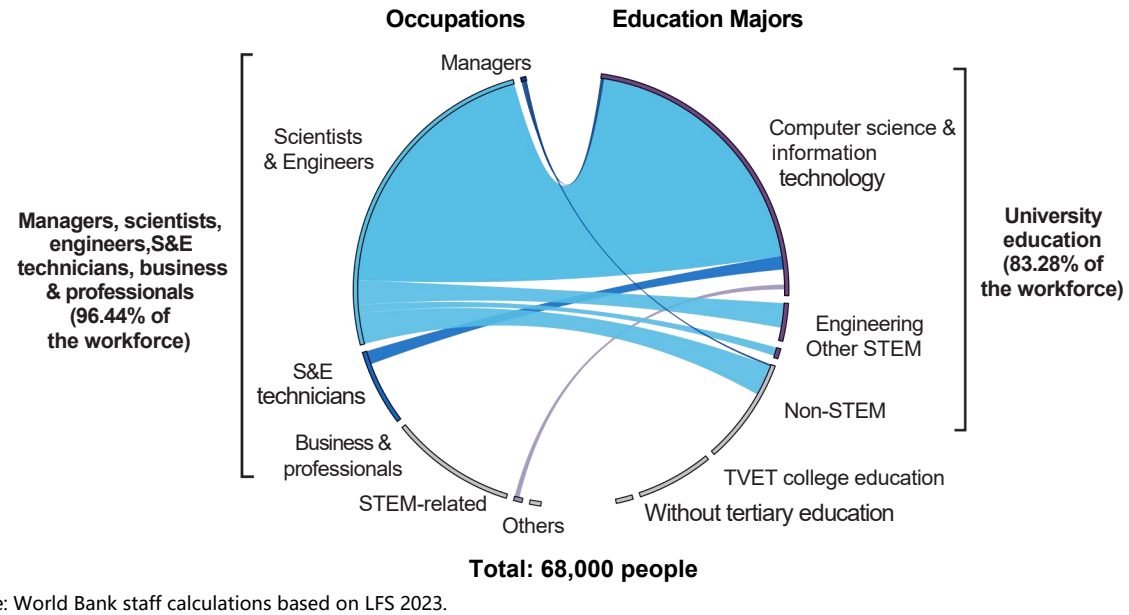
Semiconductors are simultaneously among the most technology-, capital-, and knowledge-intensive industries, with the demand for top talent rising steeply as moving up the value ladder. Section 2 opens by measuring just how steep Viet Nam's talent climb must be: it documents the knowledge- and skill-intensity of semiconductor design, and then traces the widening gap between today's modest ATP workforce and the much deeper, broader capabilities required to scale up back-end design, leap to front-end R&D, and move into advanced packaging.

The diagnosis in this section provides a clear picture of the talent frontier Viet Nam must cross to realize its semiconductor ambitions. Using national labor force data, firm and university in-depth interviews for Viet Nam, and jobs and skills requirements from globally leading semiconductor firms in the leading foreign markets, the section maps four archetypal talent gaps – each linked to the market opportunities identified in Section 1 – and highlights where quantity, relevance, and frontier-level quality are most binding. The section also explores how AI is altering the extensive and intensive margins of demand, how aging may constrain future talent supply, and why future innovation ecosystems will require not only engineers but also startup founders and enabling talent.

2.1. No chips without chipmakers: jobs prospect

The most advanced machines or generous tax incentives will not sustain a semiconductor industry in the absence of talent – a skilled workforce of scientists, engineers, technicians, and business and professionals, entrepreneurs, and managers. This is evident globally especially for the science and engineering (S&E) workforce: semiconductor firms worldwide are grappling with talent shortages. The issue is a mismatch – in quantity, quality, and specific skills.

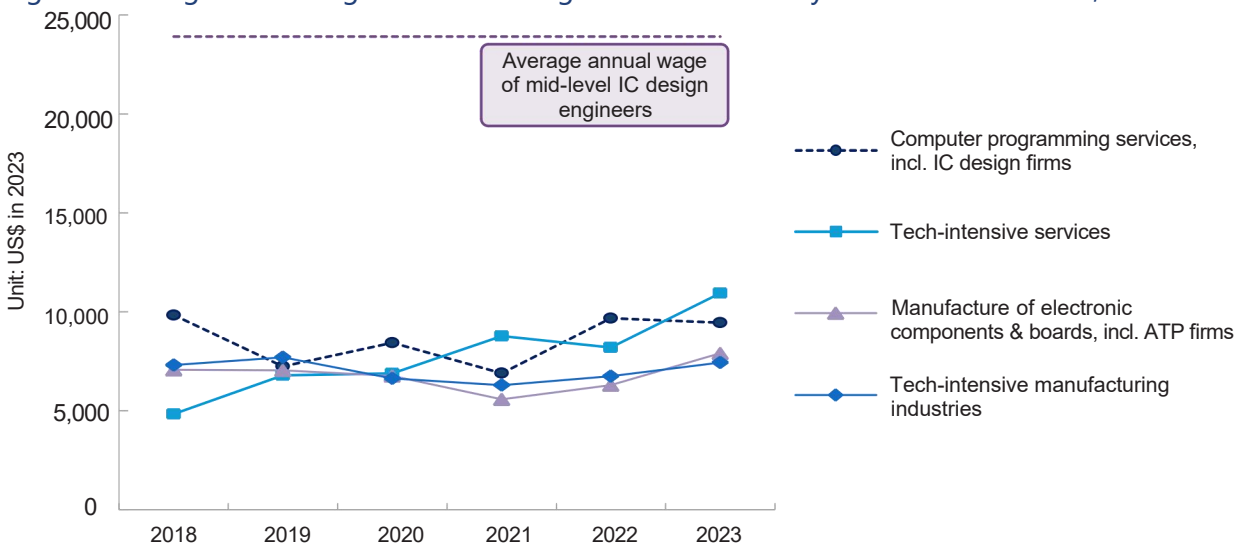
Figure 7. Occupations and majors of the existing workforce in Computer programming services (incl. IC design firms)



Source: World Bank staff calculations based on LFS 2023.

Note: The sample includes female workers aged 20-55 and male workers aged 20-60.

Figure 8. Average annual wage of mid-level engineers in Viet Nam by industries and services, 2018-2023



Sources: World Bank staff calculations based on LFS 2018-2023, ERI SalaryExpert.

Note: Tech intensity is based on OECD taxonomy. Mid-level engineers are aged 27-35 with minimum 04 years of experience.

Semiconductor roles are highly knowledge- and skill-intensive, particularly in the design segment. Data on Viet Nam's workforce underscores this point: nearly 83 percent of workers in computer programming services, which include nearly all semiconductor design firms, hold a university degree or higher, and nearly 90 percent of them have skilled jobs as managers, scientists and engineers, as well as high-skilled technicians (Figure 7). As with the broader sector of computer programming services, nearly all semiconductor design positions are high-skill jobs requiring advanced STEM education and specialized expertise. Assembly and test operations employ a larger share of technicians and mid-skilled workers, but even within this segment, the shares of workers with university degrees are also higher than the national average of manufacturing sectors.

These steep skill requirements translate into a significant wage premium for semiconductor talent. Engineers and specialists in this industry – especially those in design services – are among the best-paid tech professionals in Viet Nam, reflecting the high returns to their skills. For instance, a mid-level engineer in computer programming services in Viet Nam, which includes semiconductor design firms, has consistently earned substantially more than peers in other industries (Figure 8), underscoring the strong demand for these competencies. Wage premiums for mid-career engineers in ATP firms, proxied by the broader manufacturing of electronics, are less robust but still consistently higher than the average across all firms or in medium or low-tech-intensive firms.

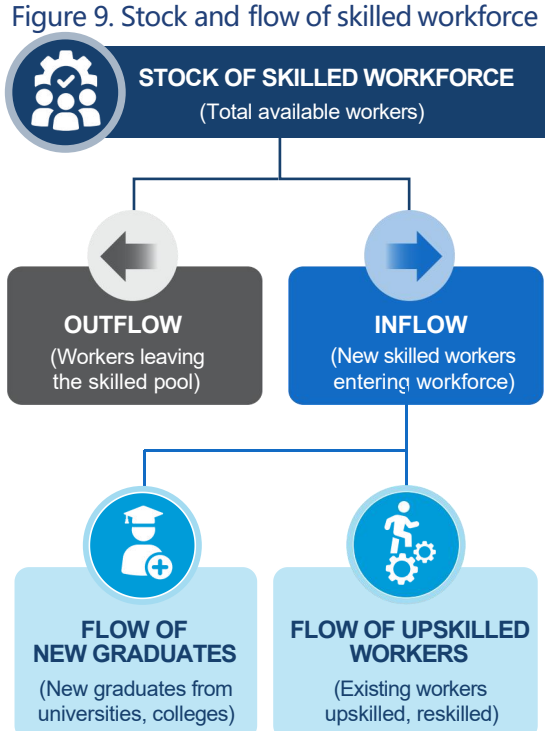
2.2. Four archetypes of talent gaps: today and tomorrow's needs

Viet Nam's semiconductor ambitions face four archetypal talent gaps with each successive scenario demanding deeper specialization, broader skill sets, and more advanced training than the last. These range from the status quo (meeting today's domestic industry needs) to three future-looking scenarios: substantially expanding back-end design activities, moving from back-end to front-end design, and advancing into advanced packaging. These gaps are identified and presented corresponding to the market opportunities in Section 1.

In essence, the status quo scenario addresses today's talent needs, while the remaining scenarios are tomorrow's needs if Viet Nam climbs the value ladder. The first two gaps benchmark demand within Viet Nam's existing industry, using the Labor Force Survey (LFS) and jobs requirements by semiconductors firms in

Viet Nam. Demand for skilled workers for front-end design and advanced packaging comes from jobs requirement in overseas markets. Specifically, for Scenario 3, they are leading front-end design firms in the US, Taiwan (China), South Korea, and Israel, accounting for 50 percent global market shares; and firms in China, Taiwan (China), and Malaysia for advanced packaging (See Annex 4 for full description).[15] It should be noted that the three aspiring scenarios are not mutually exclusive – pursuing front-end design and advanced packaging simultaneously would compound and multiply the talent constraints.

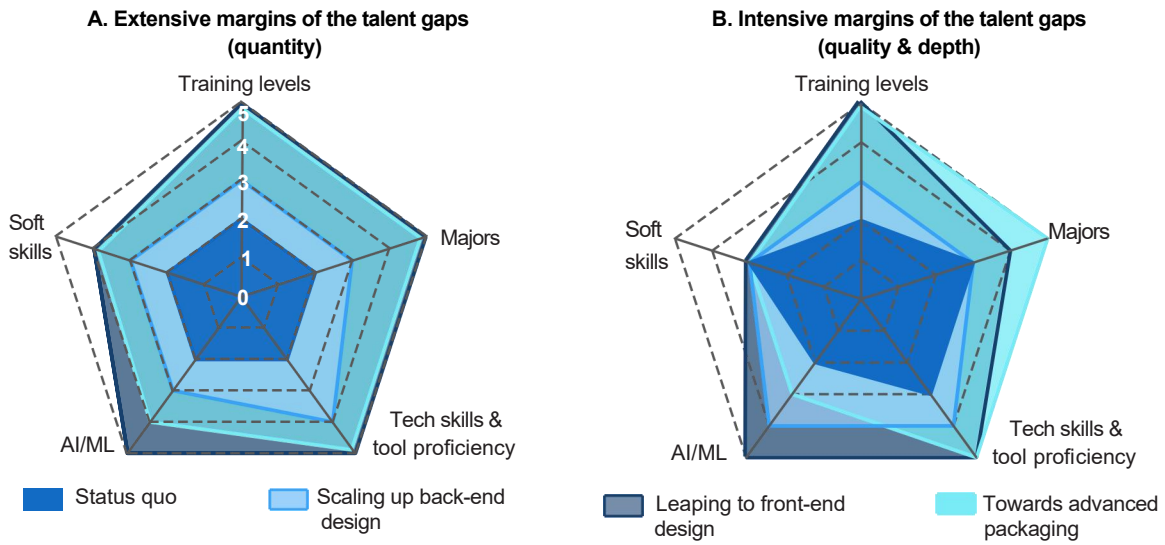
Figure 9. Stock and flow of skilled workforce



For each scenario, the talent gap is diagnosed across key dimensions of skills and training: (i) the level of education and training required; (ii) the fields, majors, and specialization of study in demand; (iii) technical skills and tool proficiency; (iv) capabilities in software, including AI/ machine learning (ML); and (v) professional "soft" skills and work-readiness. For the specific skills dimensions – technical, soft skills, and professional expectations described below – the discussion are limited for entry positions with less than 2 years of experience – most relevant for universities (skills demand for experienced engineers provided in Annex 5).

The intensity of gaps along these dimensions for each scenario become increasingly challenging (shifting from blue to light blue/turquoise and dark navy) as Viet Nam targets more advanced roles in chip design and packaging (Figure 10). Crucially, the gaps affect both the stock of the existing skilled workforce already in the industry and the flow of new graduates entering the workforce (Figure 9).

Figure 10. Extensive and intensive margins of the talent gaps



Source: World Bank staff compilation based on scenario assessments.

Note: Scale=1-5 with increasing challenges/ difficulties.

[15] This number excludes the IC design segment within Samsung Semiconductor, Intel Corporation, and TSMC, as these firms typically do not disclose revenue breakdowns by specific segments of the value chain.

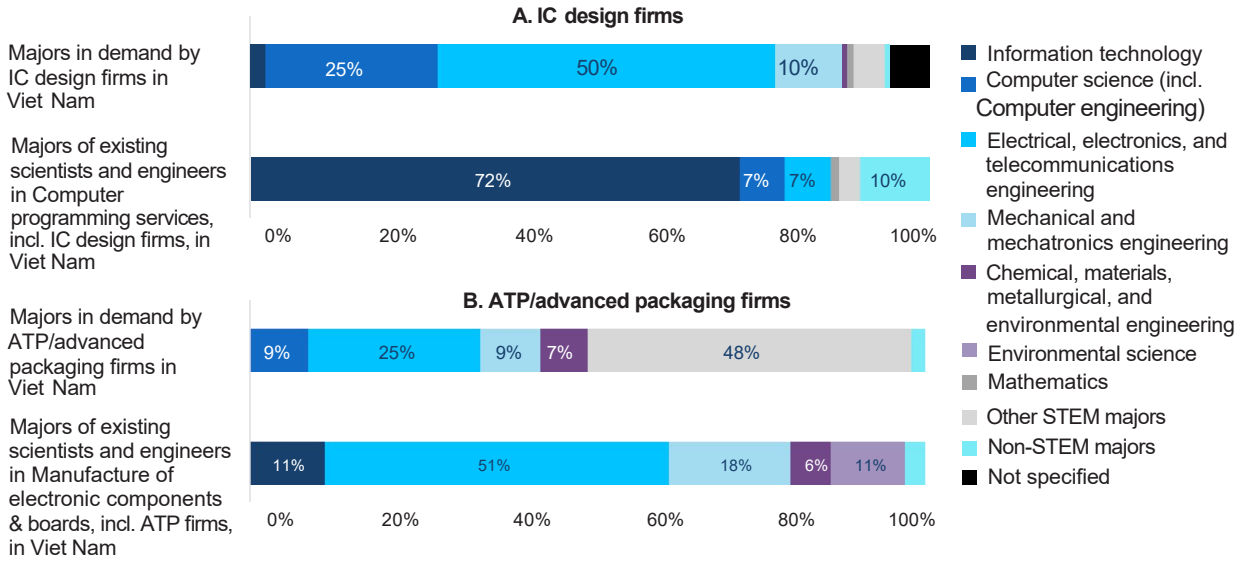
2.3. The status quo scenario: supply-demand skills alignment

Addressing the talent gap in this scenario is the first step to ensure the current base of the industry is on solid footing. Even in this status quo scenario – with Viet Nam focused on ATP and limited back-end design – there is a noticeable mismatch between industry demand and the potential pool of the skilled workforce. The skills gap fortheATP segment is benchmarked between the existing pool (supply) of the skilled workforce working in the broader umbrella industry of manufacturing of electronic components and boards, which includes semiconductor ATP firms, and the existing demand by semiconductor ATP firms currently operating in Viet Nam. Similarly, the skills gaps for backend IC design are the gaps between the talent pool in the computer programming services, which include semiconductor IC design firms, and the demand by design firms in Viet Nam (See Annex 4).

First, there is a misalignment of majors between the current stock and demand for engineers and scientists in IC design: too few design engineers with specialized electronics backgrounds and too many with more general IT backgrounds (Figure 11, Panel A). Specifically, the most immediate talent pool for IC design firms comes from the umbrella computer programming services, which includes semiconductor design firms, has nearly three-fourths of the workforce with IT specialization, whereas employers mainly seek graduates in Electrical Engineering (EE, about 52 percent) and Computer Science Engineering (CSE, 24 percent).

Second, for the assembly/packaging segment, there is an education-level gap in the talent pool for the ATP workforce versus firms' demand: only about 8 percent of workers in the manufacture of electronic components and boards, which includes all semiconductor ATP firms, have a university degree, yet nearly 50 percent of current engineering job openings in that segment require at least a bachelor's degree (Figure 13). Here one sign of relief is the mix of majors in the workforce (dominated by electronics and mechanical engineering) more closely matches employer needs (Figure 11, panel B). In short, even today's modest demand for chip talent is not fully met – Viet Nam's talent pipeline has room to improve in aligning training quantity and relevance – fields of study, specializations, and skills – with industry needs.

Figure 11. Majors of existing scientists and engineers in semiconductor firms vs. current demand by firms in Viet Nam



Sources: World Bank staff calculations based on LFS 2023, job requirements from semiconductor firms operating in Viet Nam.

2.4. Scaling up back-end design: expanding the talent base and aligning skills

The second scenario represents a value-chain upgrade where Viet Nam significantly expands its back-end IC design activities while solidifying its ATP presence. Back-end chip design work is more skill-intensive and would require scaling up the quantity of engineers with appropriate training, as well as better alignment of their skills to design work. The talent gap in this case is benchmarked between the existing pool (supply) of the skilled workforce in both electronics manufacturing and computer programming services and the demand for them by design firms already operating in Viet Nam when the country significantly scales up back-end design (See more in Annex 4).

Scaling up back-end IC design requires a workforce with substantially higher education levels. At present, the talent stock of the computer programming services has about 83 percent of employees with a university degree or higher (Figure 7). Moving up the value chain into design, even back-end design, while maintaining a strong foothold in ATP will demand many more engineers with at least a bachelor's degree, to meet the skills gaps in Scenario 1 plus the demand for talent by design firms of which nearly 90 percent S&E staff are university-degree holders (Figure 12, panel B). It will also require that those engineers have the right specializations and skills.

Regarding specialization, scaling up back-end design means increasing the share of graduates from electrical/electronic engineering and related fields. Currently, the domestic S&E supply for chip design skews toward IT majors, as noted in Scenario 1. In addition, engineers will need deeper familiarity with EDA tools and chip-specific software. Today's entry-level designers in Viet Nam often have only basic exposure to such tools; scaling up back-end design capability calls for strengthening university curricula and training in applied circuit design skills (e.g., use of schematic capture, simulation software, printed circuit board – PCB design, etc.).

Ultimately, Viet Nam must produce more engineers with a solid STEM degree and relevant design tools proficiency – along with incremental improvements in the alignment of majors and technical training. Notably, at this stage the frontier skill demands by existing design firms, like advanced research or AI/ML capabilities, remain limited. Communication and teamwork skills are important for any engineering role, but the soft skill gap is not as pronounced – new graduates mainly need to be work-ready in a conventional office/lab setting and able to integrate into design teams, similar to current expectations.

2.5. Leaping to front-end design: deepening and expanding the talent pool

This scenario, when Viet Nam moves from back-end to front-end design, opens a deep qualitative gap - essentially a jump from an engineering workforce to an R&D-capable workforce – i.e. moving from doing implementation and support design work to doing full-chip R&D, architecture, and advanced logic/circuit design. It combines a need for a higher level of training, broader and deeper skills (spanning additional domains and advanced tool usage), incorporation of AI/software skills, and stronger research and innovation-oriented mindsets. This is the talent profile needed if Viet Nam aspires to attract or grow fabless design companies and participate in the cutting-edge design segment. The analysis below documents the gaps between skill demand by design firms in Viet Nam versus that of the US, Taiwan (China), South Korea, and Israel (See Annex 4 for the list of firms).

Qualitatively, this gap is far more challenging than the previous ones: it's not just about more, but about a different caliber of talent. The educational level requirement would rise substantially – leading design firms in front-end segments often expect a Master's or PhDfor R&D roles (Figure 12, panel C). About one-third of entry postings in leading markets require advanced degrees, compared to a negligible share (only approximately 4 percent MSc/PhD) in Viet Nam's current design job market of computer programming services. Thus, Viet Nam's largely bachelor-level talent pool in the design segment would need a significant upgrade with a much higher share of postgraduate-qualified specialists to compete at the front-end.

The sought-after majors and fields would also broaden. While electronics and computer engineering remain core, front-end design pushes into areas like material science, applied physics, and mathematics, which are increasingly relevant for chip architecture, new materials and processes, and new device research. This means talent from science departments (physics, chemistry), not just traditional engineering, would be in greater demand to drive innovation.

On the technical skills front, Scenario 3 exposes a wide gulf even for fresh graduates with less than two years of experience, posing challenges to Viet Nam universities in equipping their graduates with advanced skills (Table 4). Advanced chip design roles demand deeper expertise in subjects like microarchitecture, analog and mixed-signal design, and hardware-software co-design. Fresh graduates in leading markets are expected to have hands-on experience with complete chip design flows and specialized methodologies that Vietnamese graduates typically lack. For example, a new engineer in markets like the US, South Korea, and Israel might be expected to work from register transfer level (RTL) through to graphic database system II (GDSII) (the full design-to-tapeout flow), optimize designs for power and performance, and run complex verification suites – whereas a new engineer in Viet Nam today might only be familiar with writing basic RTL or doing unit-level verification tasks. Similarly, proficiency with the latest EDA tools and programming skills is a differentiator. In short, the bar for technical tool proficiency and practical experience is significantly higher.

Figure 12. Education levels of existing workforce vs. demand by IC design firms in Viet Nam and foreign markets

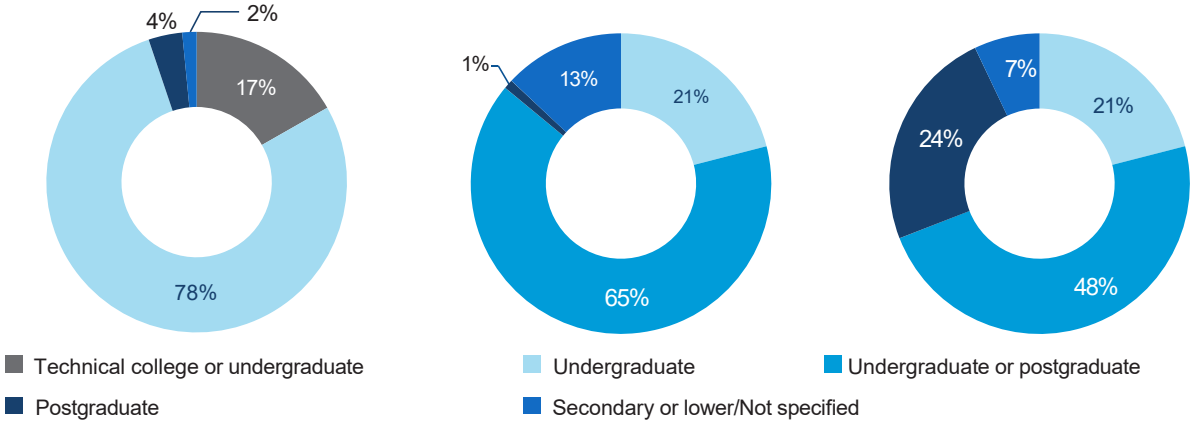


Table 4. Demand for skills of fresh graduates with less than 2 years of experience by IC design firms

Skills groups	Skills	By IC design firms in Viet Nam (mostly back-end design)	By IC design firms in foreign markets (US, Taiwan [China], South Korea, and Israel) (mostly front-end design)
Technical Skills	Digital Design	Fundamental digital logic skills	Advanced digital IC design (ASIC, RTL)
	Analog & Mixed-Signal Design	Basic transistor-level analog design Basic understanding of mixed-signal circuits (op-amps, PLLs, LDOs)	Extensive transistor-level analog design Comprehensive mixed-signal circuit integration, advanced high-speed analog circuits, ADC/DAC, SerDes, PLLs, advanced PHY design
	System Architecture	N/A	Strong emphasis on system-level architecture, including integration, interfaces, and signal integrity
	Fabrication & Process	Basic semiconductor fabrication processes knowledge	Deep understanding of advanced fabrication processes (FinFET, CMOS, BiCMOS)
	Verification & Testing	Basic transistor-level simulations Circuit-level verification	Advanced verification methodologies (UVM, SystemVerilog) ASIC verification & validation
Tool Skills	EDA/CAD Tools	Basic familiarity with Cadence, Synopsys tools Circuit simulators (Hspice/XA)	Advanced tool proficiency (Synopsys, Cadence complete suite) Field-programmable gate array (FPGA) emulation, debugging tools
	Scripting & Automation	Basic scripting skills (Python, TCL, Perl) Basic Linux environment usage	Advanced scripting and programming skills (automation and flow scripts) (Python, Perl, TCL, Unix Shell) Deep Linux proficiency
	PCB Tools	Limited PCB design experience mentioned; basic knowledge of layout entry tools	Advanced PCB design skills, high-speed PCB, signal integrity, power integrity, EMC compliance
AI/ML Skills	Data Handling & Automation	Basic Python scripting (general data handling)	Deep-learning models (TensorFlow, PyTorch) Generative AI (LLM, GAN)
	AI Applications	N/A	Computer vision/image processing AI optimization for chip performance
	AI Frameworks & Tools	N/A	Explicit use of advanced AI frameworks (TensorFlow, PyTorch)
Language & soft skills	Language Proficiency	Good English communication	Advanced English proficiency (technical documentation, presentations)
	Teamwork & Collaboration	Teamwork, interpersonal skills, self-motivation	Teamwork and collaboration (cross-functional, geographically diverse teams)
	Work Flexibility, Mindset, Leadership	General adaptability	High adaptability & independence Strong target-oriented and analytical mindset Strong leadership skills

Sources for Figure 12 and Table 4: World Bank staff analysis based on LFS 2023, job requirement from IC design firms (Synopsys Inc., Marvell Technology, Nvidia Corporation, MediaTek Inc., Renesas Electronics, Broadcom Inc., Qualcomm Inc., Ampere Computing, Faraday Technology, and Qorvo, Inc.); IP firms (Arm Holdings plc), and IC design job requirements from Intel Corporation, Samsung Semiconductor, and TSMC, accessed in March-April 2025. Data for Renesas Electronics, Ampere Computing, Faraday Technology, and Qorvo, Inc. includes only Viet Nam job requirements.

Note: The workforce includes those with university education and aged 22-35, inclusive.

Crucially, demand for AI and ML proficiency emerges as a new frontier in this scenario. In leading chip design firms, AI/ML capabilities are increasingly expected even of hardware engineers – for instance, using ML for circuit optimization, or developing AI accelerators – whereas Vietnamese firms have yet to incorporate AI/ML into job requirements for design engineers. This represents a cutting-edge skills gap: to engage in front-end design, the next generation of Vietnamese engineers would need significant exposure to and experience with AI/ML concepts (for example, applying neural networks to optimize chip layouts or using AI in EDA tools) that currently are not part of the standard skill set.

Finally, the soft skills and professional expectations in a front-end R&D environment are elevated. Domestic employers today value English proficiency and teamwork, but overseas R&D teams place greater emphasis on things like independent research ability, cross-cultural collaboration, and creative problem-solving leadership from an early-career engineer. New hires in global firms may be expected to proactively drive parts of a project, liaise with international colleagues, and adapt quickly to ambiguous, cutting-edge problems.

2.6. Towards advanced packaging: deepening and expanding the multidisciplinary talent pool

This scenario introduces a multi-disciplinary talent challenge that is distinct from chip design and the talent gap is simultaneously broad, deep, and multidisciplinary connected. The talent gap corresponds to Viet Nam moving up from traditional ATP to advanced packaging – adopting cutting-edge packaging and testing technologies such as 2.5D/3D integration, wafer-level packaging, etc. Moreover, bridging will require not only more graduates in each relevant field, but also a new level of cross-functional expertise and process-oriented professionalism. It underscores an institutional challenge: training programs and industry will need to collaborate in unprecedented ways to produce talent with such a blend of skills.

On the education level side, a greater proportion of the workforce would need formal degrees compared with traditional ATP. Advanced packaging firms in leading markets typically require a much higher share of engineers (83 percent with university degrees or above) than Viet Nam's current ATP firms (nearly 47 percent) (Figure 13). Yet today nearly 20 percent of Viet Nam's potential pool of ATP skilled workforce from the broader electronics manufacturing industry has tertiary education (technical and vocational education and training – TVET colleges and university degrees combined). Bridging this gap means upgrading the workforce's educational attainment – more bachelor-level process engineers, materials engineers, and even postgraduates for R&D in new packaging materials and techniques (indeed a small but non-negligible fraction of advanced packaging roles in top markets require MSc/PhD).

Just as important is realigning the fields of study that feed into packaging. Advanced packaging sits at the intersection of multiple fields – mechanical, materials, chemical, electrical, and computer engineering, plus applied sciences. In particular, expertise in mechanical/mechatronic engineering is critical for dealing with thermal stresses and precision assembly (and foreign firms' demand for this major is proportionally higher – e.g., about 32 percent of postings) (Figure 14). Similarly, materials science and chemical engineering have become much more prominent due to the need for specialized substrates, adhesives, and fabrication processes in modern packaging.

The technical skill gaps for entry levels with less than two years of experience in advanced packaging are twofold (Table 5). First, there is a gap in the depth of specific process knowledge and tool expertise. Domestic ATP operations currently emphasize general production skills – running surface-mount technology (SMT) machines, maintaining equipment, basic quality control, etc. In contrast, advanced packaging operations require familiarity with cutting-edge semiconductor equipment and processes (for instance, wafer bumping, chip stacking/bonding techniques, high-precision lithography for packaging, advanced testing methods) and the ability to integrate and troubleshoot these processes. Engineers in leading markets are often expected to

have hands-on experience with IC packaging and test equipment, advanced metrology tools for sub-micron quality assurance, and a strong grasp of semiconductor process integration. Second, akin to the design gap, AI/ML capabilities are becoming relevant in advanced manufacturing environments as well. Foreign advanced packaging firms require skills in data analytics and ML – for example, using AI to optimize production yields or predictive maintenance on equipment.

Figure 13. Education levels of existing workforce vs. demand by ATP/advanced packaging firms in Viet Nam and foreign markets

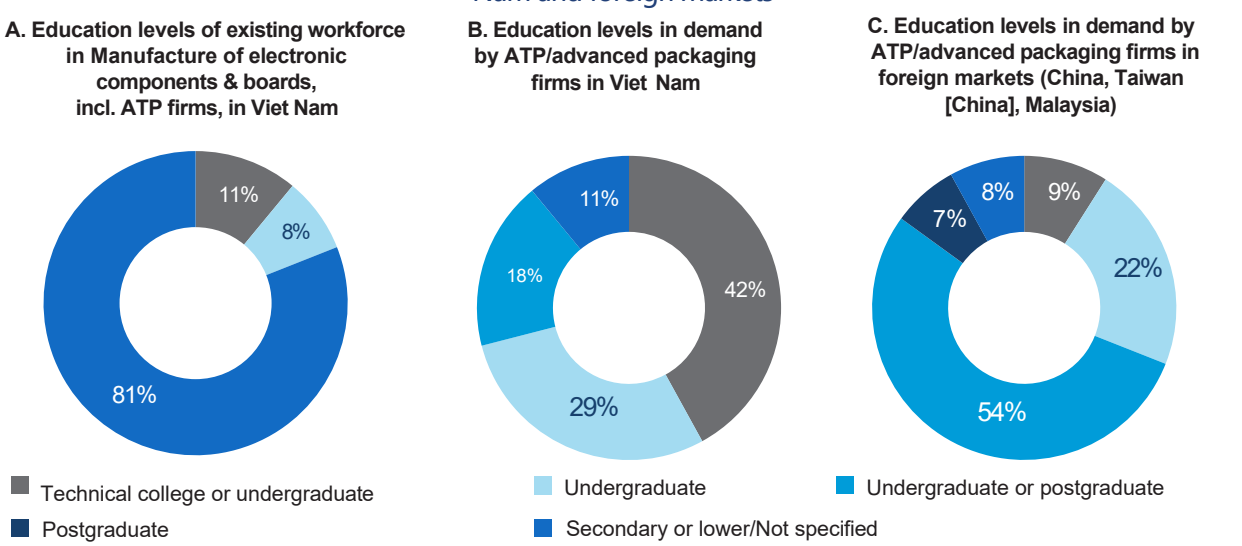
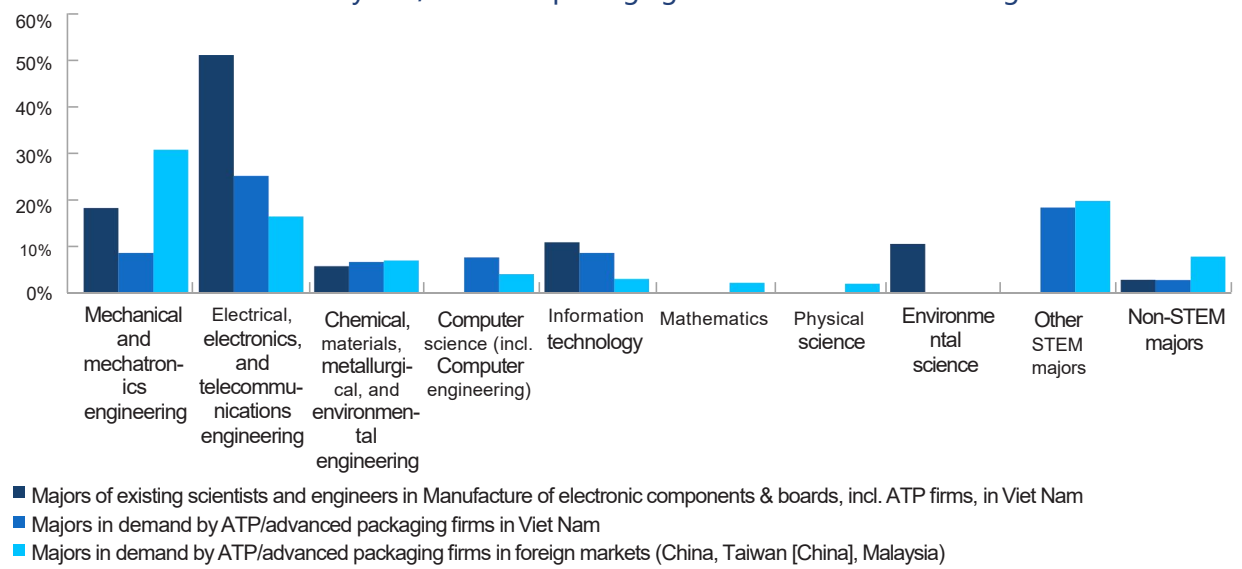


Figure 14. Majors of existing scientists and engineers in Manufacture of electronic components & boards vs. demand by ATP/advanced packaging firms in Viet Nam and foreign markets



Sources for Figures 13 and 14: World Bank staff calculations based on LFS 2023, job requirements from ATP/advanced packaging firms operating in Viet Nam and foreign markets (Amkor Technology, Siliconware Precision Industries, Advanced Semiconductor Engineering, Powertech Technology Inc., JCET Group, and Hana Micron Vina), and ATP/advanced packaging job requirements from TSMC and Intel Corporation, accessed in March-April 2025.

Note: The workforce includes those with university education and aged 22-35, inclusive.

In terms of professional and soft skills, the advanced packaging scenario poses an interdisciplinary coordination challenge. Because the work merges elements of mechanical engineering, materials science, electronics, and computer control systems, effective collaboration across specialties is crucial. This means future engineers must be adept at teamwork across disciplinary boundaries – a skill set that siloed training may not foster.

Table 5. Demand for skills of fresh graduates with less than 2 years of experience by ATP/advanced packaging firms

Skills groups	Skills	By ATP/AP firms in Viet Nam	By ATP/AP firms in foreign markets (China, Taiwan [China], Malaysia)
Technical skills	Electronics/ Electrical	SMT lines, electronic production processes, automatic machines, PCB assembly	Semiconductor-specific equipment (IC packaging/testing, front-end and back-end equipment, wafer-level chip scale packaging –WLCSP), bumping processes)
	Quality Management	Process improvement, quality control, defect analysis, staff training	Semiconductor quality assurance, process engineering in semiconductor packaging/testing, yield optimization, quality control
	Environmental and Safety Systems	Heating, ventilation, and air conditioning (HVAC), wastewater treatment, air compressors, electricity, air conditioning, chemical safety	Certifications in Class A/B air pollution, wastewater treatment, environmental, social, and governance (ESG) management, occupational safety and hygiene certificates
	Mechanical Engineering	General equipment operation and maintenance, environmental facilities	Semiconductor equipment maintenance (physical vapor deposition – PVD), wet process equipment, electroplating machines, etchers, photoresist strippers)
	IT Infrastructure	General IT infrastructure knowledge, server/storage management	Network system configuration, cybersecurity, manufacturing execution system (MES), enterprise resource planning (ERP) (Oracle/PROMIS), smart query systems
	Design Engineering	General package design knowledge, basic substrate understanding, tolerance interpretation	Advanced IC packaging design, substrate and PCB layout design, bumping, fan-out wafer-level packaging, yield improvement
Al, ML		N/A	Data analysis, ML, deep learning, computer vision applications, usage of toolkits (TensorFlow, OpenCV, Cognex, Halcon, Keras)
Tool skills	MS Office	MS Office	MS Office
	Computer-Aided Design (CAD) Tools	EDA (Cadence), CAM, AutoCAD (basic usage, 2D drafting)	AutoCAD (advanced, 2D and 3D design), Cadence Allegro (advanced PCB design), ANSYS (simulation software for stress, thermal analysis)
	Programming Tools	Basic database management, general programming languages	C#, Python, R, SAS, MATLAB, Java, SQL, VBA, ASP.NET
	Control Systems	SCADA and CCR operation (preferred)	Programmable logic controller programming, advanced MES systems
Language & soft skills	Language	English communication	English communication
	Soft Skills	Interpersonal skills	Teamwork, effective communication, coordination, project management; problem-solving, analytical skills
	Shift Flexibility	Basic flexibility for shifts (not strongly emphasized)	Strong emphasis on mandatory shift rotations (day/night shifts)

Sources: World Bank staff analysis based on job postings from ATP/advanced packaging firms (Amkor Technology, Siliconware Precision Industries, Advanced Semiconductor Engineering, Powertech Technology Inc., JCET Group, and Hana Micron Vina) and ATP/Advanced packaging job postings from TSMC and Intel Corporation, accessed in March-April 2025.

2.7. A future-proof talent pool: AI, entrepreneurship, and demographic aging

AI reshaping talent gaps in semiconductor design

AI-driven automation in back-end design is shrinking extensive margin of the talent demand with fewer routine roles, but increasing demand for AI-augmented and high-value-added roles. This trend could particularly affect countries that hoped to grow via routine back-end services. Recent advances in AI for EDA are automating many "back-end" chip design tasks that traditionally required large teams of engineers. Tools like Synopsys DSO.ai and Cadence Cerebrus use ML to explore design spaces and optimize layouts, completing tasks that used to take weeks of manual effort. Synopsys reports its AI has been used in 100+ chip tape-outs (including at Samsung and SK Hynix) and delivered productivity gains in block-level physical design.[16] [17] AI's ability to take over repetitive tasks means companies can achieve the same design goals with smaller teams. In other words, automation is shrinking the extensive margin of talent demand for routine design roles.

Meanwhile, the intensive margin demands higher productivity and new skill requirements with rising productivity and skill per engineer. AI boosts efficiency but also changes job profiles: engineers must now oversee and guide AI tools, interpret their results, and handle the complex corner cases AI can't solve. The role of a back-end designer, for instance, is shifting from manually crafting layouts to curating AI-driven solutions and refining the design constraints. In practice, this requires combining traditional domain knowledge with new AI/ML tool competencies. Companies like Synopsys and Microsoft foresee an "AgentEngineer" paradigm where human engineers collaborate with AI agents, necessitating workflow changes and knowledge management to fully leverage AI's potential.[18]

Front-end design remains human-driven and specialty-intensive in contrast to back-end implementation. Front-end design roles – which include system architecture, microarchitecture (high-level functional design), logic/RTL design, and analog/mixed-signal circuit design – are not readily automated by current AI.[19] These tasks involve creative architectural decisions, complex algorithmic trade-offs, and intuition built on physics and circuits expertise. Analog IC design in particular is famously difficult to automate, lacking clear-cut optimization heuristics, so human designers rely on deep intuition and iterative refinement that AI tools have yet to replicate effectively. Even in digital front-end design (like defining a new processor's architecture or writing an optimized RTL block), AI can assist, but it cannot replace the architect's system-level understanding or the creative insight needed to invent novel solutions.

Consequently, the talent demand at the front-end remains for highly skilled engineers, often with postgraduate degrees and research experience. In the US, Taiwan (China), South Korea, and other leading chip design hubs, nearly one third of front-end design engineers have Master's or PhD degrees, and top firms commonly require advanced degrees for R&D roles. This reflects the intensive knowledge requirement – domains like chip architecture or analog/RF design draw on cross-disciplinary expertise (e.g., computer science, electrical engineering, physics, mathematics) that goes beyond routine engineering curricula.

16 Wilson, R. (2023). AI-assisted chip design continues to catch on. Retrieved from https://www.electronicdesign.com/technologies/eda/article/21261479/electronic-design-ai-assisted-chip-design-continues-to-catch-on

17 Synopsys. (2024). Copilot: Generative AI for chip design. Retrieved from https://www.synopsys.com/blogs/chip-design/copilot-generative-ai-chip-design.html

18 Synopsys. (2024). AgentEngineer technology: Transforming engineering workflows. Retrieved from https://www.synopsys.com/blogs/chip-design/agentengineer-technology-transforming-engineering-workflows.html

19 Synopsys. (2024, April 30). Analog IC design tools: SNUG panel. Retrieved from https://www.synopsys.com/blogs/chip-design/analog-ic-design-tools-snug-panel.html

Entrepreneurship for thriving home-grown semiconductor firms

A thriving chip industry requires not onIy chip designers and process engineers but aIso entrepreneurs who can turn technicaI breakthroughs into viabIe businesses. The ability (both the skill and mindset) of an engineer to turn ideas into impactful innovations, whether within a startup or larger company, is key to maintaining a competitive advantage in today's knowledge economy. Entrepreneurial training equips students to harness technology not just to build products but to solve real-world problems with meaningful social impact. It also empowers researchers to learn how to move innovations from the lab to the market, accelerating the pathway from discovery to application. Globally, leading engineering universities offer standalone or integrated entrepreneurial courses to not only build a strong startup culture among students and faculty members but also to foster multidisciplinary collaborations and develop leadership, creativity, communications, and problem-solving skills.

However, founders - often scientists and engineers - must aIso be supported by compIementary taIent and enabIing services. The rise of Taiwan (China), for example, was built on a "talented workforce, mostly engineers," and at one leading fabless firm, roughly 80 percent of employees have advanced engineering degrees. Mainland China now boasts over 3,600 IC design companies. India, meanwhile, is training 85,000 chip designers under its Chips-to-Startup program to fuel its nascent fabless ecosystem. The industry's future also hinges on skilled managers, project operations specialists, supply chain and sales teams, and IT support staff to translate innovation into production and business success. Industry experience shows leading chip companies explicitly cultivating nontechnical support functions (e.g., dedicated tracks for marketing, sales, finance) alongside technical teams.

Demographic aging and the pressures on semiconductor talent

Demographic shift after 2036 is shrinking Viet Nam's youth Iabor pooI. An aging workforce can pose to innovation capacity – even tech-leading nations are asking who will design the next generation of chips as their core engineering cohorts grow older (McKinsey 2024).[20] Viet Nam's current "golden population" period will end around 2036, when the country transitions into an aged society (World Bank 2021).[21] [22] The share of seniors will rise quickly thereafter, among the fastest demographic aging rates globally. A post-2036 aging population could slow the growth of Viet Nam's skilled workforce just as demand for tech talent is surging, posing a risk to the country's semiconductor and tech ambitions.

Semiconductor design roIes skew younger, demanding fast cycIe, and intensive skiIIs. Key semiconductor jobs – especially front-end chip design, verification, and other R&D-intensive engineering roles – tend to be held by younger professionals, due to rapid innovation cycles and intensive skill requirements. Sustaining cutting-edge chip design capacity requires continuously infusing young talent versed in the latest tools and techniques. This youth-skewed workforce profile underpins innovation but is vulnerable if the supply of young engineers diminishes over time.

[20] McKinsey & Company. (2023). How semiconductor companies can fill the expanding talent gap. Retrieved from https://www.mckinsey.com/industries/semiconductors/our-insights/how-semiconductor-companies-can-fill-the-expanding-talent-gap

[21] VNExpress. (2024, March 3). Aging before prosperity: Vietnam's challenge. Retrieved from https://e.vnexpress.net/news/perspectives/aging-before-prosperity-vietnam-s-challenge-4829652.html

[22] Tuổi Trẻ News. (2024, April 20). Vietnam likely to end golden population period in 2036: Experts. Retrieved from https://news.tuoitre.vn/vietnam-likely-to-end-golden-population-period-in-2036-experts-10377677.htm

There are international warning signs for aging engineers in Taiwan (China), South Korea, and the US. In the US, for example, one-third of semiconductor workers are already aged 55 or above, raising concerns about replacing retirees in coming years.[23] South Korea's major chipmakers have even introduced programs to retain veteran experts beyond the usual retirement age so that "aging engineers with outstanding expertise are not forced to retire," reflecting worries about a shrinking young talent pool. Taiwan (China) likewise is grappling with a dwindling supply of young engineers amid the world's lowest fertility rate and a rapidly aging population.[24]

Demographic aging likely has differing impacts on chip design versus manufacturing. Workforce aging will likely affect chip design and chip manufacturing segments in distinct ways. IC design (front-end engineering, research and development) is highly creativity-driven and requires continual skill renewal. By contrast, chip manufacturing can benefit from the deep experience of long-tenured engineers and technicians; veteran process engineers play a key role in maintaining quality and mentoring younger staff. However, some production roles are physically demanding or involve round-the-clock shifts that older workers may find difficult, suggesting that manufacturing too will require steady recruitment of younger workers.

Bottom line: balance today's versus tomorrow's talent needs

To close the skills gap for today and be ready for tomorrow, Viet Nam must walk a fine line between deepening foundational skills and enabling dynamic specialization. First, a robust core of STEM graduates – especially in electronics, computer engineering, and applied sciences – is the foundation. But as the country moves up into more R&D-intensive design and advanced packaging segments, a second layer of skills must emerge: deeper technical expertise, stronger analytical and research capacity, and an innovation mindset. Second, the nature of semiconductor work is shifting – not just across value-chain stages (ATP versus front-end design), but also with AI changing how chips are designed and built. Back-end roles may become more accessible thanks to AI tools, but front-end, analog, and architectural design remain intensely human. Not all engineers need to become researchers, but the system must cultivate enough high-caliber scientists and specialists to anchor the frontier. Similarly, not all engineers and scientists will become entrepreneurs, but the system must enable and support them when needed.

"Industry can't grow faster than the talent behind it" - Viet Nam's challenge is to ensure talent growth not only meets but also leads industry development and demand. As Viet Nam moves forward, these findings underscore a clear imperative on the supply side of talent. The next section turns to the country's higher education and training system – the foundation of its talent pipeline – and examines how it can expand and adapt to produce the specialized workforce that the industry will need in the future.

---

23 McKinsey & Company. (2024). How semiconductor companies can fill the expanding talent gap. Retrieved from https://www.mckinsey.com/industries/semiconductors/our-insights/how-semiconductor-companies-can-fill-the-expanding-talent-gap

24 Wang, R. (2024, February 14). Taiwan's semiconductor talent shortage. Retrieved from https://thediplomat.com/2024/02/taiwans-semiconductor-talent-shortage/

3. THE TALENT SUPPLY, UNIVERSITY TRAINING AND INNOVATION CAPACITY

Viet Nam's higher education and training system is the foundation of its semiconductor talent pipeline - but it is under pressure to deliver more specialized and innovative graduates at scale. This section synthesizes key opportunities and challenges to the talent supply and the training and R&D capacity of the higher education system. Viet Nam s ambition of moving up to more R&D-intensive semiconductor segments hinges not just on a broad base of engineers and technicians, but on frontier talent the researchers, inventors, and postgraduates who drive innovation. This section diagnoses Viet Nam s performance in innovation talent, pinpoints root causes of its R&D talent gap, and draws implications for moving up the value chain in chip design and advanced packaging. These observations are drawn from national labor and enrollment data, survey results from leading tech universities, and rapid assessments of curriculum, research, and infrastructure conditions especially at Vietnam National University Ho Chi Minh City (VNUHCM) and its network of universities.[25] The findings point to a dual challenge: expanding and deepening semiconductor and talent supply (especially in chip design, advanced engineering, and applied R&D), while improving system-level incentives for innovation and alignment with industry.

3.1. The stock and flow of semiconductor skilled workforce

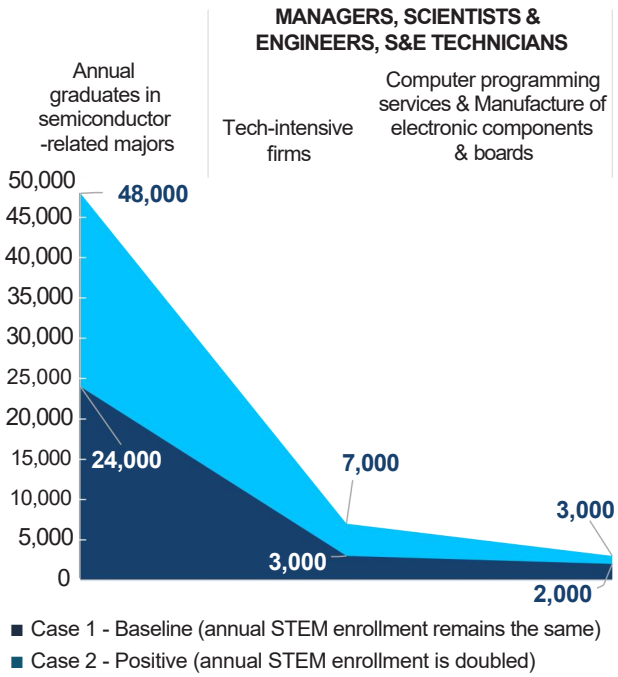
Viet Nam has built a substantial base of STEM talent and continues to expand its pipeline of technical graduates. Among young professionals aged 22–35, roughly 560,000 hold university degrees in STEM fields in 2023 – a sizable talent stock providing a strong foundation. The annual flow of new STEM talent is also rising rapidly, with undergraduate STEM enrollment growing by nearly 10 percent per year from 2019 to 2023 outpacing trends in many advanced economies. For comparison, South Korea and Germany have seen their STEM graduate cohorts shrink by around 0.2 0.3 percent annually, and even the European Union (EU) and China recorded only 1 3 percent annual growth.[26] Approximately 30 percent of Viet Nam s undergraduates are enrolled in STEM, exceeding the EU average and approaching levels seen in leading semiconductor economies.

However, this expanding pipeline has not yet translated into a strong semiconductor talent pool with reasons lying on both sides of the labor market. On the demand side, employment in technology-intensive industries and services remains modest, limiting absorptive capacity; on the supply side, constraints in university quality, research capacity, and specialization continue to limit the volume and caliber of frontier-level engineers. Based on 2023 data from 17 leading science and technology universities, about 24,000 students graduate each year in majors relevant to the semiconductor value chain (Figure 15). Yet even with rising enrollment, only around 3,000 graduates annually are estimated to enter semiconductor-related jobs in design, engineering, or advanced manufacturing. In short, while the base of STEM talent is growing, the effective pipeline into the semiconductor workforce remains narrow. Unlocking this potential will require closing both the demand gap by generating more high-skill jobs and the supply gap by expanding higher education capacity and raising the technical depth and specialization of its graduates.

[25] VNUHCM member universities provide information include: University of Science (HCMUS), University of Technology (HCMUT), University of Information Technology (UIT), International University, Institute for Nanotechnology (INT) and Center for Innovative Materials and Architectures (INOMAR).

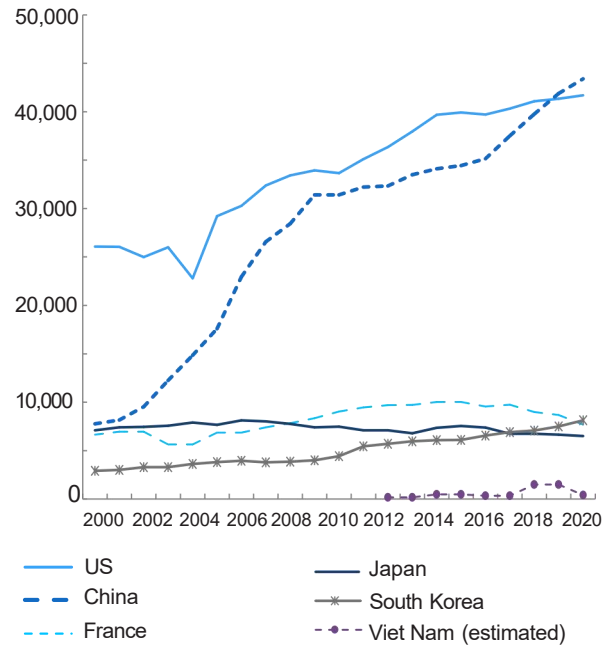
[26] Eurostat; Korea Statistical Yearbook of Education, 2019-2024; Educational Statistics Yearbook of China, 2019-2022.

Figure 15. Projection of annual flow of graduates in semiconductor-related majors and their workplace



Source: World Bank staff calculations based on universities' 2024 enrollment plans. The projection is based on annual enrolment in semiconductor-related majors in 17 universities[27] in the national program for semiconductor workforce development.

Figure 16. Doctoral degrees awarded annually in S&E



Sources: US National Science Foundation, Viet Nam Science and Technology Report.

Table 6. R&D personnel in Viet Nam, 2013-2023

Year	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
R&D personnel (full-time equivalent) (thousands)	73.09	67.29	68.87	60.10	66.46	72.46	75.13	71.98	59.08	66.24	80.87
Labor force share (%)	0.136	0.125	0.127	0.110	0.121	0.131	0.135	0.131	0.117	0.128	0.154

Source: World Bank staff calculations based on National Statistics Office of Viet Nam, LFS 2013-2023.

Note: R&D personnel are all persons engaged directly in R&D (such as researchers as well as those providing direct services for the R&D activities – R&D managers, administrators, technicians and clerical staff) (OECD 2015). Number of employees are converted to full-time equivalents (FTEs) using the FTE conversion factor.

Moreover, Viet Nam's output of top talent with postgraduate degrees in relevant fields is very limited, with a stagnating pool of quality master's and PhD-level graduates, who are critical for R&D intensive segments and for the next generation of faculty (Figure 16). Many students choose to go straight to the industry after a bachelor's degree duetothe high cost and limited scholarships for graduate school. Those who do pursue PhDs often go abroad and many do not return. Over the past 10 years, the absolute number and proportion of the R&D workforce (full-time equivalents – FTE) in the total labor force – have remained virtually unchanged (Table 6). For semiconductors-related sectors, it is estimated that fewer than 70 PhDs in electrical, electronics, and telecommunications engineering graduate domestically per year.[28] Even in leading institutions as VNUHCM, this is also seen in the small number of PhD and master's students that participate in a semiconductor-related research group (Figure 22). Overall, this limits the country's capacity for high-quality postgraduate education and innovation in advanced technologies.

[27] We excluded Military Technical Academy due to a lack of data.

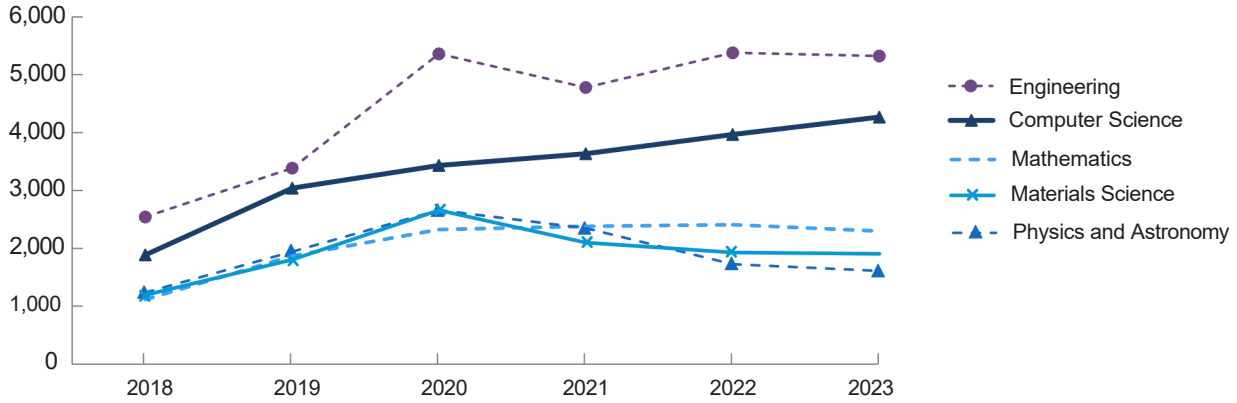
[28] World Bank staff calculations based on MOET (2024). The rough estimate is based on the total number of enrolled PhD candidates of about 323 people in electrical, electronics, and telecommunications engineering in 2023, assuming a dropout rate consistent with recent trends of about 15 percent.

Combined with the discussion on the market demand and gaps with the current supply, the bottom line is Viet Nam faces two key demand-supply challenges: (i) expansion of capability – ensuring that the talent pool is broad, deep, and interdisciplinary and they are equipped with the necessary specializations, technical skills, and experience, to meet today's and tomorrow's needs; and (ii) expansion of opportunities – fostering the creation of sufficient high-skill roles in the domestic market and better pathways for university graduates to enter those jobs.

3.2. Semiconductor-related research & development outputs

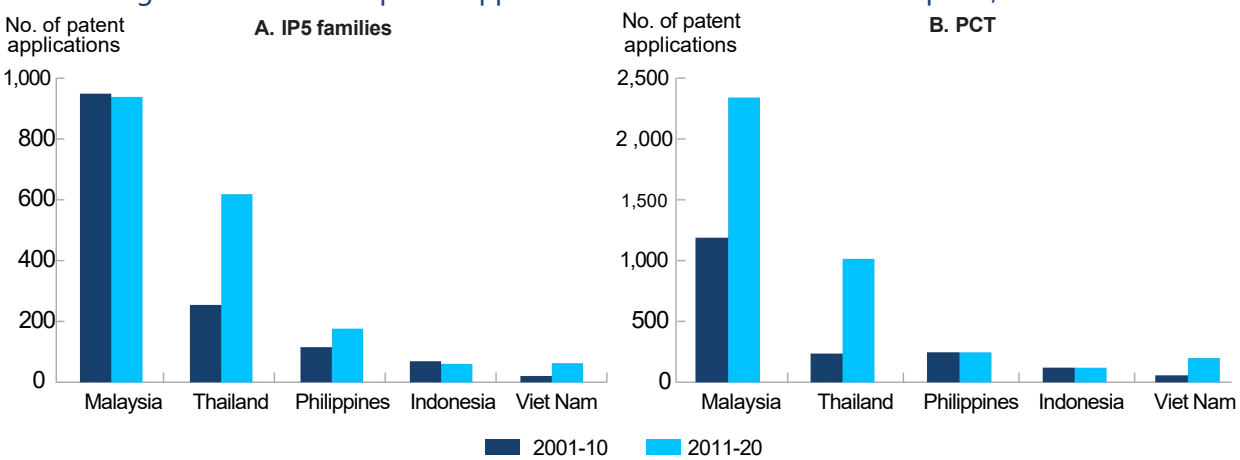
In recent years, Viet Nam's research output in engineering and computer science, the two most relevant fields for semiconductors, has increased significantly. The number of scientific publications, particularly in international journals, has risen sharply, reflecting an improvement in research capacity. Notably, scientific publications in the engineering field continue to lead, while the computer science field has also seen strong growth. These two fields account for 50 percent of Viet Nam's total international publications (Figure 17). At the same time, the volume and quality of research output still lag behind regional peers and leading economies. Viet Nam produces about 11 scientific articles per billion Gross Domestic Product (GDP), versus 48 for South Korea and 40 for Singapore, and its research H-index remains well below that of Malaysia or Thailand.

Figure 17. The five majors with the highest number of international publications in Viet Nam, 2018-2023



Source: MOST (2024).

Figure 18. Number of patent applications in Viet Nam and selected peers, 2001-2020



Source: OECD (2024b).

Note: Patent Cooperation Treaty (PCT) patents. Fractional counting method, inventor's country of residence and priority date used. IP5 patent families refer to patents that have been filed in at least two IP offices worldwide, one of which among the five IP offices (namely the European Patent Office, the Japan Patent Office, the Korean Intellectual Property Office, the US Patent and Trademark Office, and the State Intellectual Property Office of the People's Republic of China). Fractional counting method, inventor's country of residence and priority date used.

Viet Nam has one of the lowest patent application densities in the region with very limited contribution by universities. From 2011–2020, Vietnamese inventors filed virtually no patents under the top international patent families (IP5), whereas Malaysia filed hundreds, and even the Philippines managed around 20 percent of Malaysia's count (OECD 2024b, Figure 18). Patent filings by Vietnamese universities rose from approximately 50 in 2016 to nearly 200 in 2023, yet they account for only about 22 percent of domestic patent applications and less than 1 percent of PCT-standard filings. Likewise, technology-transfer revenue averages just 4.3 percent of university income, versus over 20 percent at leading Asian peers – indicating limited commercialization of research. In semiconductor-related patents, Viet Nam and Indonesia effectively filed zero under IP5 in the past decade (OECD 2024b). Singapore – the global and regional leading innovation hub – and Malaysia, a regional emerging semiconductor hub, vastly outpaces Viet Nam on these metrics, with far more patents per capita and per GDP in both general and semiconductor fields.

3.3. Pillars of higher education training, research, and innovation

Academic excellence and research clusters

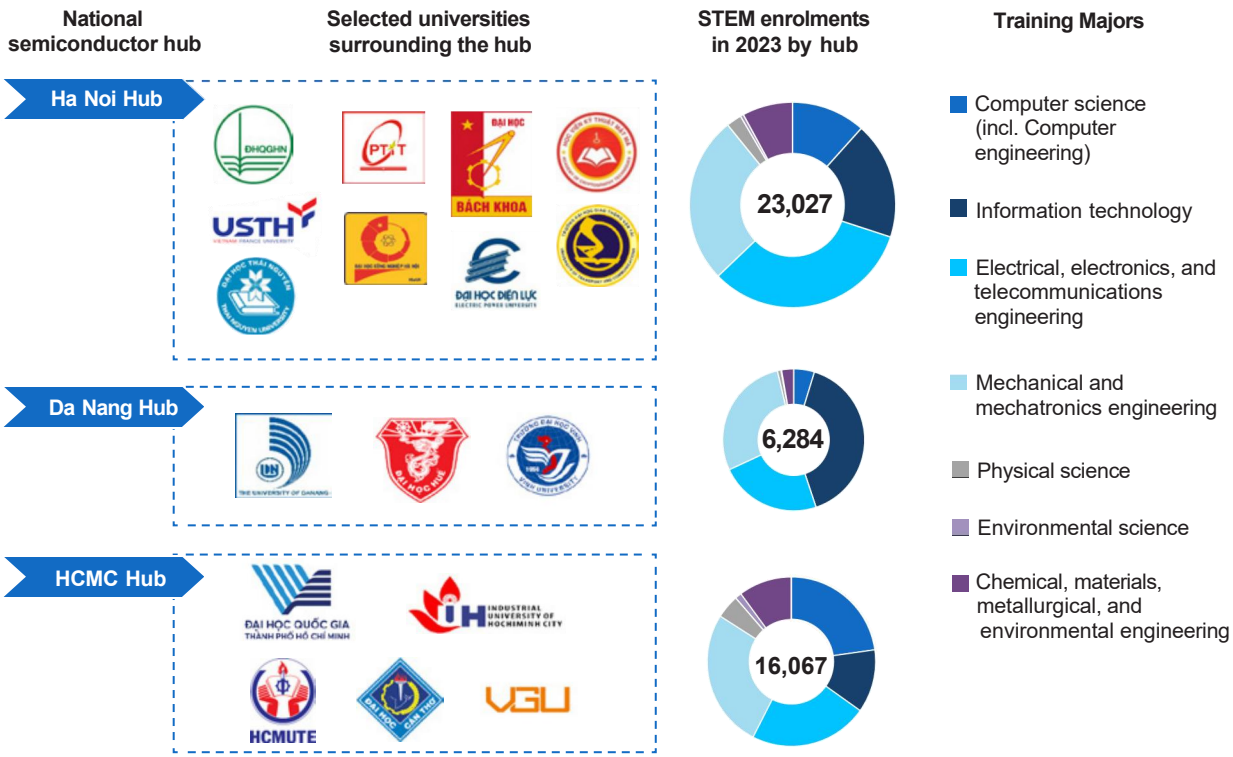
Viet Nam's universities have seen significant improvements in the global ranking in the last five years. Hanoi University of Science and Technology (HUST) remains the public flagship, anchoring the 401-450 bracket of QS Engineering & Technology globally and 67 in South-East Asia. Vietnam National University, Hanoi (VNUHN) is in the global 451-500 group for the same category with four already inside the top-400. In the South, VNUHCM has also broken into the 901-950 tier of the QS World University Rankings 2025 and its flagship petroleum-engineering programme is in the top 100. These three universities are also within the top 1000 in the Times Higher Education (THE) Engineering global ranking. The cumulative effect is a doubling of Vietnamese universities appearing in global STEM top 1000 – from four in 2020 to eight in 2025 – driven by increasing investment in publication output, international collaborations, and English-medium PhD pipelines.

At the same time, Viet Nam has yet successfully developed any regional emerging science and tech clusters and none of its universities has broken into the global top 100 in S&E. As discussed below, the key factor is the shortage of PhD-level faculty and research mentorship. With under one-third of faculty holding a PhD, and heavy teaching loads, universities struggle to build "centers of excellence" in fields like advanced electronics or materials. Top talent often goes abroad (brain drain), and those who stay face resource constraints. Viet Nam has yet to develop a critical mass of internationally recognized scientists in semiconductor-related disciplines. This thin academic elite translates to fewer breakthroughs and makes it harder to attract global R&D partnerships.

Training programs: curriculum, key majors and specializations

There are positive developments in linking training programs to the market needs and international standards. Flagship institutions have started updating curricula following international standards and partnering with industry. For example, VNUHCM member universities jointly developed a new specialized microelectronics curriculum framework in 2024, as part of the VNU–industry collaboration (Figure 21). University of Technology, a member of VNUHCM, launched a talent program in IC Design, which targets the top performing students and provides them access to quality courses and well-equipped labs. Meanwhile, companies like Synopsys and Faraday have offered short courses and donated labs at universities. These efforts are steps in the right direction – updating course content, injecting real-world projects, and increasing resource-sharing across universities. Impact will be stronger if these positive initiatives are scaled nationwide.

Figure 19. STEM enrolment in 2023 by education majors in selected universities in Viet Nam



Source: World Bank staff calculations based on universities, 2024 enrollment plans.

A few top universities have strong undergraduate electronics programs; however, industry recruiters note that graduates' skill sets vary widely by university. Foundational knowledge in math, physics, etc. is generally strong (Vietnamese students do well in theory), but applied skills (like project-based learning using modern lab equipment or EDA software) are relatively weaker due to resource constraints in universities. Moreover, one university's graduates may be strong in embedded software but weak in analog design, while another's might be vice versa. Uneven preparation means companies cannot assume a baseline skill level, increasing the cost of evaluating and retraining new hires from each institution.

While key training programs, i.e., electrical/computer engineering, mechatronics, etc., are available, until recently, few undergraduate training programs had specialization in semiconductors. Most students in electronics or computer engineering had only one or two courses touching on chip design or fabrication. This is starting to change – e.g., HUST and VNUHCM have introduced microelectronics majors or very-large-scale integration (VLSI) design tracks – but such programs are still nascent and not being offered at scale. In addition, AI and ML are still limited in curricula – both as tools to enhance teaching and learning, and as subjects of study critical to the growing AI-driven high-tech industries (Figure 20). The breadth and foundation of STEM programs is there, but the focus on the technical skills that meet the semiconductor industry's current and future demands on fresh graduates is lacking.

Faculty: training and research capacity

A critical piece of educational capacity is the quality and quantity of faculty, and Viet Nam faces a faculty qualification gap in high-tech fields. Simply put, there are not enough PhD-holding, research-active faculty in electronics and semiconductor-related subjects. The percentage of PhD-holding faculty in Viet Nam is approximately 32-33 percent. At the Faculty of Electrical and Electronics Engineering at HCMUT, the ratio is 49 percent. This share is significantly low when compared with 100 percent and 94 percent for similar programs at Taiwan's National Tsing Hua University and Malaysia's Universiti Teknologi, respectively. Heavy teaching loads further strain faculty capacity – many spend most of their time teaching large undergraduate classes, with little

time for curriculum development or research. The lack of research funding exacerbates this (discussed below under incentives).

The publication rate per faculty member is relatively low across universities. For instance, the University of Da Nang (UD), one of the three largest universities in Viet Nam, could only meet the minimum standard set by the Ministry of Education and Training (MOET) on the publication rate of 0.7. In VNUHCM, the rates vary significantly, ranging from 0.24 to 2.69. To address this, VNUHCM has introduced several policies to promote publications in international journals. These include providing allowances and financial aid to academic staff to attend international conferences, funding the organization of SCOPUS-indexed international conferences, and awarding bonuses for published articles.

The postgraduate bottleneck at the doctoral level is particularly linked to faculty capacity and vice versa. Since many faculty members either lack a PhD or do not lead active research, they are limited in their ability to supervise doctoral students – creating a vicious cycle of low PhD output and constrained academic capacity within the universities. This underscores the critical need for Viet Nam to increase its pool of highly trained faculty to support the expansion of advanced training and research.

Female representation in semiconductor and STEM related fields

Gender representation in Vietnamese universities shows a relatively equitable overall student enrollment, with 54 percent of students being female. However, women are underrepresented in STEM fields, making up less than 30 percent of the total students. In terms of research outputs, only one in four authors in Web of Science and SCOPUS -indexed journals UD were female in 2020, which increased to one in three by 2024. At VNUHCM, the share of female authors reached 43 percent in 2024, up from 41 percent in 2020. Several policies have been implemented to promote research and publication by female lecturers, including converting scientific research hours to teaching hours with a weight of 1.2 for female researchers, and providing flexible research work arrangements for pregnant researchers and those with young children or elderly parents requiring special care.

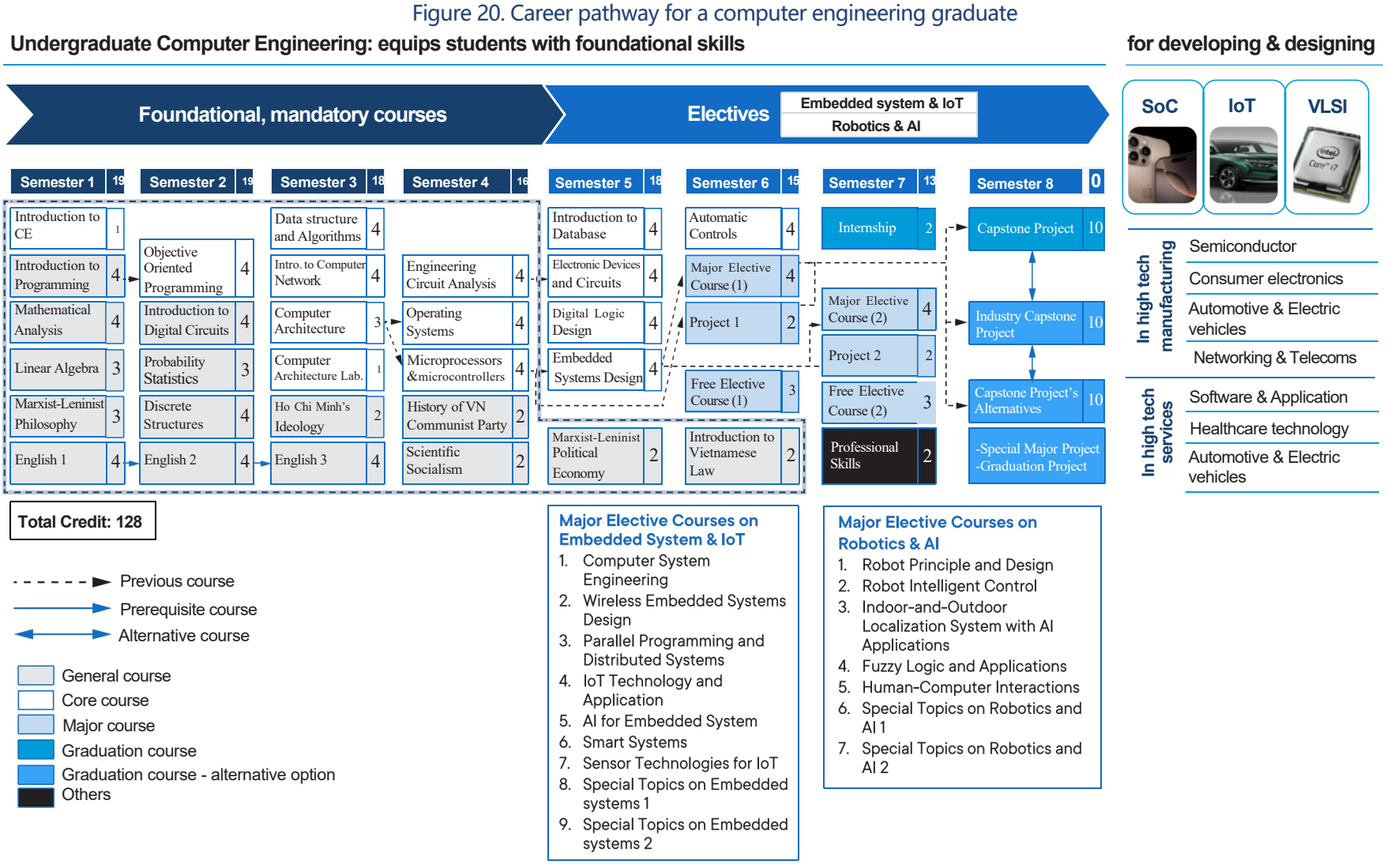
University–industry linkages in training, research and innovation

On the one hand, all major universities have established technology transfer offices, innovation and/or startup support centers to facilitate closer linkages with the industry. These innovation centers also join forces to form the Viet Nam Network of Higher Education Innovation and Entrepreneurship Centers (VNEI). It is a nationwide network of innovation-and-startup centers located in Vietnamese universities, coordinated by the National Innovation Center (NIC). Embedding more innovation and entrepreneurship components (entrepreneurship courses, business plan competitions, incubators, etc.) in engineering programs can cultivate more well-rounded talent who might create the next Vietnamese chip design startup.

At the same time, collaboration between academia and industry in Viet Nam is ad hoc and limited. Few joint labs or co-funded R&D projects exist between universities and semiconductor firms. While some companies (e.g., Synopsys, Cadence) have donated EDA software or set up training labs, these initiatives are isolated. There is no systemic program of industry-sponsored professorships, cooperative research centers, or large-scale internship/thesis programs tying students to enterprise R&D.

Consequently, technology transfer is very low. During 2018–2023, 85 percent of the value of all tech-transfer contracts in Viet Nam was generated by FDI firms, rather than domestic university–firm linkages. Vietnamese universities on average derived only about 4 percent of their revenue from science & technology services in recent years. The lack of structural partnerships (consortia, innovation hubs, co-supervised graduate research, etc.) leaves universities researching in silos, while FDI companies remain hesitant to locate R&D centers in Viet Nam (preferring to rely on in-house R&D elsewhere). This fragmentation prevents the "triple helix" of university–industry–government from taking shape in the semiconductor sector.

Figure 20. Career pathway for a computer engineering graduate



Source: VNUHCM, University of Information and Technology.

Figure 21. A positive development atVNUHCM

Observations: Positives - entry points for scaling

On the Right Track

Curricula modelled off world class engineering institutions

- VNUHCM member universities (MUs) jointly developed curricula framework for specialized programs
- VNU350 Project: Recruit approximately 350 talented scientists in the 2024-2030 period

Focus on internships, project-based learning, and senior year capstone projects

Cross-university linkages

- Existing resource-sharing policies, including faculty sharing across MUs, blended/online learning, and students taking classes at other MUs

VNUHCM Innovative Entrepreneurship Center for startup incubation and tech transfer connects VNUHCM's MUs & research institutes to the startup ecosystem

- VNUHCM's VUDP project funds the construction of a research and innovation center

National Assembly Regula This new regulation will significantly enhance and promote commercialization of research (e.g., innovation safety net to incentivize faculty)

Growing industry engagement

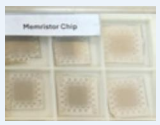
- Guest lectures, research funding, software sharing, EDA tools, internships, training programs (varied across MUs)
- PFIEV telecom lab @ HCMUT, FPT software lab @ UIT, short courses by Faraday, Synopsys

Highlights

95%

Internships are required part of curricula – 95% of UIT IC Design students get internships

Marvell sponsoring lab and course in Advanced Communications for AI Infrastructure for final year students and grad students (HCMUT, Fall 2025)

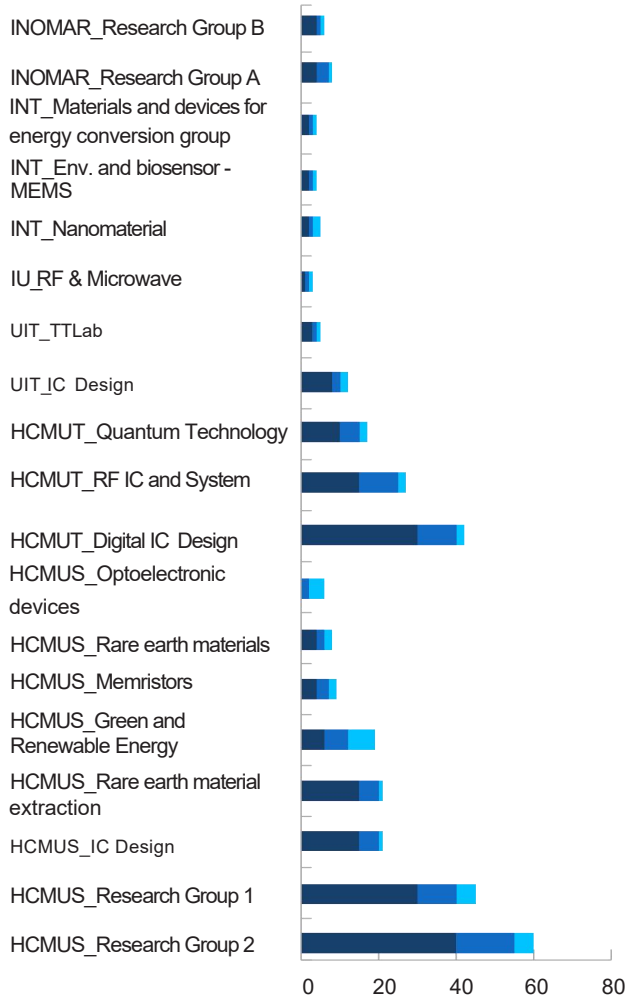


HCMUS Memristor Research Group: 5 faculty, 2 PhD, 3 MS, 4 BS – design and fab memristor, collab w Onsemi, Hyosung, VNU-Hanoi, Academia Sinica Taiwan, 70,000US$ of grants

Dedicated training / design project labs for telecom, digital signal processing, FPGAs, etc. at HCMUT

Source: World Bank staff compilation.

Figure 22. Number of types of student in each research group atVNUHCM



Source: World Bank staff calculations based on data submitted by VNUHCM' s member universities and research institutes.

3.4. University infrastructure: capital intensity of building the talent pipeline

Developing semiconductor talent isn't just about people - it's also about the tools, facilities, and technology access those people have for training, research and innovation. The semiconductor field is capital-intensive: from cleanroom labs for fabrication practice to high-performance computers for chip design, the infrastructure required to train a chip engineer or conduct chip R&D is expensive. Viet Nam currently faces significant infrastructure gaps that, if unaddressed, will hinder skill development no matter how motivated the students or faculty are.

University laboratory deficits and short-term tools access

Most Vietnamese universities lack advanced labs for electronics and semiconductor training and research, and when the labs exist, their usage might not be efficient. Many engineering departments have only basic electronics labs (sufficient for simple circuits, not for nanoscale semiconductor experimentation). There are very few cleanroom facilities in the country available for education, research, or prototyping. As a result, the research output of universities is low, and students graduate with strong theoretical knowledge but minimal hands-on experience with semiconductor processes. For example, a microelectronics student might learn about Complementary Metal-Oxide Semiconductor (CMOS) fabrication steps in a textbook but never actually see or operate deposition or lithography equipment during their studies.

Modern chip design relies on tools (from companies like Cadence, Synopsys, Siemens EDA) for simulation, layout, and verification. These EDA tools can cost tens of thousands of dollars per license annually. Top global universities have site licenses giving students access. In Viet Nam, most universities cannot afford comprehensive EDA suites. Some have partial licenses or use outdated versions. One finding was that at HCMUT, students had Cadence tools but lacked Synopsys, limiting exposure to both major platforms. VNUHCM had to rely on industry donations for certain tool access.

These gaps contribute directly to the long on-the-job training needed later for these graduates. The lack of EDA access means graduates often have not used the very software they will need in industry – an obvious skills gap. Universities like VNUHCM, where some training programs were observed to assign 3-8 students per lab station, identified facilities and equipment needs related to training and research in device physics and material science, semiconductor fabrication, and advanced packaging. However, sustainable funding has been a challenge in closing this gap. For the 2023/2024 academic year, one of the two research groups at INT received external research funding as low as US$8,000 (Figure 23, Figure 24). The launch of the VNU350 in 2024, an internal research grant program at VNUHCM, if sustained and scaled, could be a game-changer.

Low digital infrastructure access and efficiency

Although Viet Nam has made significant enhancements with respect to the digital transformation of its higher education system, challenges remain. Advancements in digital infrastructure are particularly beneficial for universities as they enable high-speed access to digital resources, cloud-based learning platforms, and research databases while also supporting the implementation of smart classrooms and virtual laboratories. In addition, High-Performance Computing (HPC) systems and data centers are critical for integrating AI/ML into teaching, learning, and research. Digital infrastructure is equally critical to improving productivity across economic sectors and fostering innovation, especially in high-tech industries. As highlighted earlier, the semiconductor industry and AI/ML are increasingly interdependent, with advancements in one driving progress in the other. Through the Vietnam University Development Project (VUDP), the VNUHCM, VNUHN, and UD are improving the campus internet network, the learning management system to support e-learning, and plan to acquire HPC systems.

Figure 23. External research funding from non-industry sources (US$)

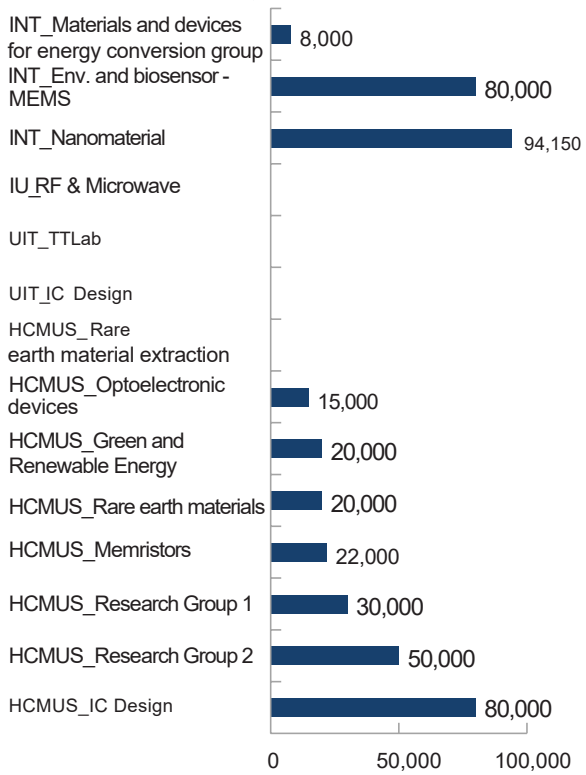
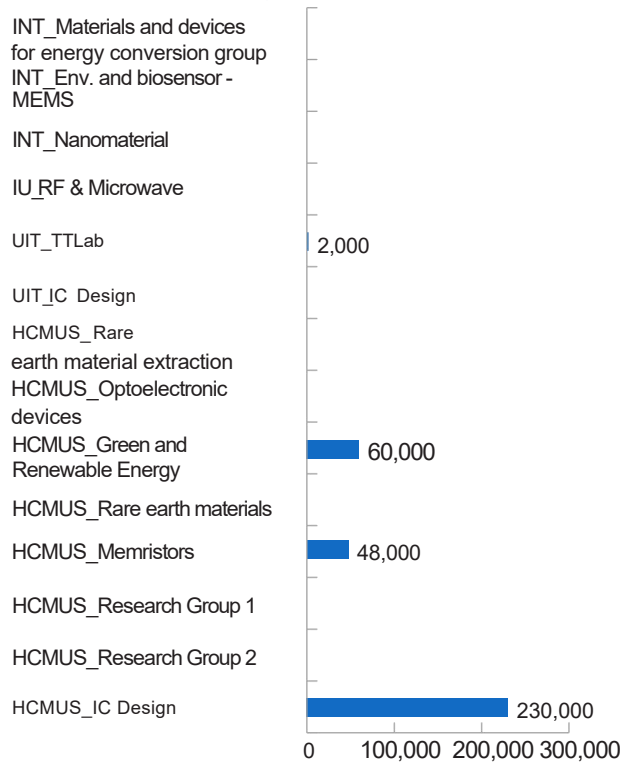


Figure 24. External research funding from industry sources (US$)



Source: World Bank staff calculation based on data submitted by the semiconductor-related research groups within the member universities and research institutes of VNUHCM.

However, Viet Nam still needs to make bolder steps, not only in acquiring enabling digital infrastructure for training and innovation but also in ensuring its efficient use, in particular, through better coordination between universities and industry. For example, Viet Nam's National Research and Education Network (VinaREN) has a backbone speed of 1-10Gbps, offers basic digital services (connectivity), and weak industry collaboration. On the other hand, Taiwan Advanced Research and Education Network (TWAREN) offers a backbone speed of more than 100Gbps, and provides value-added services, such as Cloud, Storage, AI compute, and testbeds to both universities and industries.

Missing shared facilities and infrastructure

The national scheme for National Semiconductor Technology Hubs/Centers: Viet Nam is establishing four national-scale semiconductor laboratories within its leading universities – VNUHCM, VNUHN, the City of Da Nang – and the NIC, to advance its position in the global semiconductor industry. These hubs focus on critical areas such as IC design, semiconductor materials, AI chips, and advanced manufacturing techniques. Specifically, the lab at VNUHCM will cover all stages of semiconductor design, production, packaging, and testing, while VNUHN will focus on microchip and semiconductor device production. The Da Nang City lab will focus on the design and testing of microchips in close collaboration with the UD, while the NIC will focus on design, packaging, and testing of microchips, supporting training, technology incubation, and AI applications. This initiative aims to pool resources from these top universities, research institutes, and industry partners to create a one-stop center with state-of-the-art labs (design labs, characterization labs, maybe a prototype fabrication line) and technology transfer facilities and support to strengthen collaboration between academia, industry, and government.

There are no significant domestic R&D centers or pilot lines in advanced packaging or chip design – segments where peer countries are investing heavily. Researchers must send chip prototypes abroad for fabrication and testing, causing delays and "innovation leakage." Nascent efforts exist (e.g., the NIC near Hanoi, and new labs at VNUHCM), but these are not yet at the scale needed to drive an ecosystem. Without a concentrated "hub" where academia, start-ups, and multinationals co-locate, the spillovers and network effects that power innovation remain weak. The absence of university-centric innovation parks or specialized semiconductor institutes is a structural gap.

Resource pooling and shared facilities in Viet Nam are missing or often on an ad-hoc basis. For example, although each Vietnam National University (VNU) supports a network of universities, these institutions have yet to fully leverage the significant economies of scale and shared resources that the network model can offer. The planned National Semiconductor Technology Centers – discussed above are a strong signal from the government – but it' s still in the early stages. If fast-tracked by 2026, this could significantly close the infrastructure gap by providing a place where students and firms alike work on real chip prototypes without each needing to invest millions individually.

Table 7. Infrastructure needs for research labs and facilities atVNUHCM

		HCMUS	HCMUT	UIT	INT	INOMAR
Materials Research Labs	Materials characterization lab	●			●	●
IC Design Labs	Digital IC Design Lab	●	●	●		
	Mixed signal IC design Lab	●		●		
	Radio Frequency (RF) IC design lab		●	●		
	HPC	●				
Fabrication/ Manufacturing	Cleanroom modules 10,000 and 100,000	●			●	
	Cleanroom modules 100 and 1000	●	●		●	
	Semiconductor devices characterization	●	●		●	
Advanced Packaging Labs	Advanced packaging lab	●	●		●	
	ATP	●	●		●	●
Other	Robotics & embedded systems lab (ML)	●		●		

● Existing programs require facilities currently not available
● Facility exists but lack several specialized equipment or require upgrades
● Facility exists and well equipped

Source: World Bank staff consolidation based on infrastructure assessment data submitted by the VNUHCM member universities and research institutes that focus on semiconductor related fields.

Note: Infrastructure quality varies across universities and campuses within the VNUHCM network. Updates and enhancements to infrastructure for teaching and research are needed for VNUHCM. Examples of specialized equipment needed are follows. Digital IC lab at HCMUT needs highspeed oscilloscopes, high speed logic analyzer high speed Logic Analyzers, FPGA, wave form signal generator, vector signal analyzer, IC design emulator. Characterization of devices/materials at HCMUS: apart from the need for cleanrooms, also, requires Field Emission Scanning Electron Microscope (FE-SEM), High-resolution Transmission Electron Microscope (HR-TEM), X-ray Diffraction (XRD) system, Fourier Transform Infrared (FTIR) spectrometer (FTIR), etc.

lf Viet Nam couId deveIop a centraIized repository of aIIthe avaiIabIe speciaIized equipment across the nationaI hubs and campuses, it wouId faciIitate better coIIaboration and efficient use. One university s underused equipment can be accessed by researchers or students from another university or researchers from industry. The rapid assessment at VNUHCM shows that the network of universities of VNUHCM is lacking an asset/inventory tracking mechanism. INT currently has an online platform that allows partners to reserve cleanroom equipment.

A commonIy overIooked gap is maintaining Iabs with sophisticated equipment. Universities might acquire a high-end microscope or etcher, but if it needs repairs, they lack funds or expertise to fix it, leading to idle equipment. That s why we propose every major lab investment includes a maintenance endowment or service contract for 7 10 years. This could mean training technicians and securing spare parts as part of the purchase deal. Additionally, it is important to have a model, especially for shared facilities, where maintenance fees are built into the cost of using the facility.

Link to broader Higher Education-Science–Tech–Innovation capital needs

lt is worth noting that this infrastructure chaIIenge is not unique to semiconductors. Across higher education and R&D in Viet Nam, under-investment in training facilities, labs, and equipment has been a longstanding issue. Fields like biotechnology, renewable energy, and materials science face similar gaps. The government s commitment to raising science, technology, and innovation (STI) spending to about 2 percent of GDP partly addresses this. Some of those increases should target upgrading specialized training facilities, R&D labs, and also broader innovation infrastructure.

Viet Nam's government-Ied initiatives have estabIished both physicaI and institutionaI innovation spaces, exemplified by the NIC, the VNEI network, and the VUDP. For example, the NIC has opened a flagship hub atthe Hoa Lac Hi-Tech Park – a 20,000 m² complex outfitted with prototyping labs, co-working offices, and conference facilities – to attract startups and tech firms while promoting research, technology transfer, and commercialization.[29] [30] In parallel, the VNEI connects a nationwide network of university-based innovation centers, fostering on-campus makerspaces, incubators, and collaborative labs to nurture student entrepreneurship and partnerships with industry.[31] Meanwhile, under the VUDP, major universities (such as VNUHCM, VNUHN, and UD) are upgrading infrastructure with state-of-the-art research and innovation facilities including specialized laboratories in priority fields like renewable energy, environmental technology, climate science, and high-tech agriculture.[32]

However, these innovation spaces are often not weII integrated into academic programs, research, and Iack strong connections to externaI tech hubs, incubators, and industry networks. Beyond enabling policies, technology transfer support services, and entrepreneurial skills that help drive innovation in universities, access to the right infrastructure is also important to provide hands-on experience with mechanical and digital fabrication tools, creativity, and problem-solving skills. Globally, universities increasingly have their own and/or are typically closely affiliated with external innovation facilities, such as incubation centers/hubs, accelerators, or makerspaces. In addition to the training and research labs, leading engineering programs also invest in well-staffed and well-equipped machine and tool workshops, and fab labs (with prototyping capabilities such as 3D printers, computer numerical control CNC milling, and laser cutters).

---

29 Asia Architecture and Design Awards. (2024). NIC National Innovation Center. Retrieved from https://aadawards.com/winners-2024/NIC_National_Innovation_Center-tid50

30 Vietnam National Innovation Center. (n.d.). Cơ sở Hòa Lạc – Vietnam National Innovation Center. Retrieved from https://nic.gov.vn/a/148436/CO-SO-HOA-LAC

31 Ministry of Planning and Investment. (2024, May 16). Deputy Minister Tran Duy Dong attends National Innovation Forum 2024. Retrieved from https://www.mpi.gov.vn/en/Pages/2024-5-23/Deputy-Minister-Tran-Duy-Dong-attends-National-Inno201q0.aspx

32 The World Bank. (2024). VUDP: Implementation Support Mission November 18 to 29, 2024. Retrieved from https://documents.worldbank.org/en/publication/documents-reports/documentdetail/099041525125139455

The coordination and linkages between university-level innovation centers and with the wider innovation ecosystem are also weak. For VNUHCM and VNUHN innovation centers, once construction through the VUDP is completed, it is critical that these centers are equipped with state-of-the-art facilities and technologies that support interdisciplinary collaboration, better integration into academic programs and ongoing university research, prototyping, and fabrication. Equally important is ensuring strong integration with the broader innovation ecosystem – linking the university (faculty and students) with startups, tech entrepreneurs, and industry partners. This includes going much deeper with collaborations, and also encouraging co-investment and joint management models of these centers that enable shared use, sustainable operation, and the translation of academic research into market-ready solutions.

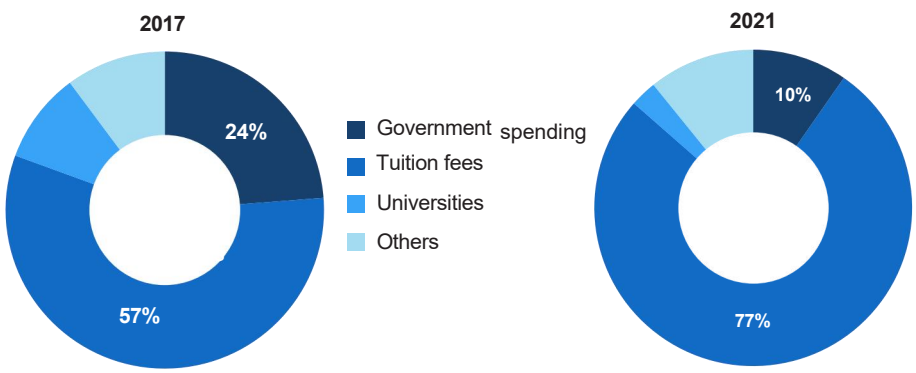
In summary, this assessment finds that Viet Nam's semiconductor workforce development program must confront the infrastructure question head-on. For an industry as semiconductors and critical technologies that Viet Nam is targeting, the talent pipeline and research output will flow as fast as the capacity of the labs, tools, and facilities that train and enable that talent. Investing in modern educational infrastructure – and innovative models like shared facilities – is as important as investing in people.

3.5. Financing and incentives for university training and innovation

Public funding for universities has not kept pace with enrollment growth, and institutions rely increasingly on tuition (Figure 25). Viet Nam's top public universities, given more autonomy, have gradually charged higher tuition and get relatively less state subsidy per student in recent years.

This has several consequences on accessibility, equity, and infrastructure. First, students shoulder more education cost, which can deter pursuing graduate studies. Many cannot justify paying for a Master's or PhD program (and forego income) when an industry job after a bachelor's is available. The opportunity cost is high, so few take the graduate path, leading to the small postgraduate numbers noted. Expanding scholarships for graduate schools (domestic and abroad) is essential to change this calculus. Second, faculty are not strongly incentivized to specialize or innovate in teaching. With limited research funding and heavy teaching loads, there is little reward for developing and renovating semiconductor training programs. Third, due to tight budgets, training labs and associated facilities at many universities are outdated or insufficient, as discussed more in the next section. Training in semiconductors requires expensive equipment (oscilloscopes, FPGA kits, cleanroom facilities for fabrication, testing and measuring, etc.). Many Vietnamese universities lack these or have only a few that students rarely get to use.

Figure 25. Sources of university income in selected public universities in Viet Nam

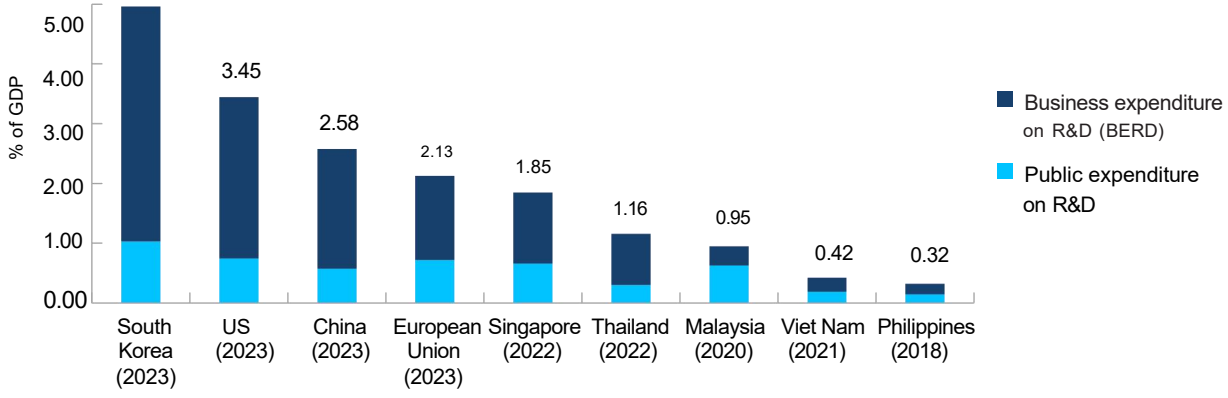


Source: World Bank (2023).

Viet Nam also under-invests in research overall with an extremely thin industrial research base. Total R&D expenditure was just about 0.4 percent of GDP in 2021, far below the 2–5 percent seen in regional peers and aspiring economies and even trailing Malaysia (Figure 26). Crucially, business R&D is only 0.2 percent of GDP – indicating that few firms conduct significant in-house innovation. By comparison, firms' R&D spending accounts for about 1.7 percent of GDP in China and 3.6 percent in South Korea. Even mid-tier ASEAN peers outspend Vietnam in private R&D spending. The weak private R&D footing means Vietnam lacks industry "pull" for advanced research and new chip technology development. Overall R&D investment remains far below the government's own targets (2 percent of GDP by 2030), and is insufficient to seed an innovation-driven semiconductor ecosystem.

Public R&D is inefficient and fragmented. Public research spending, while relatively large compared with other peers as shares of total R&D spending, is not translating into commensurate outputs. Government R&D outlays (expenditure) spread thinly across many ministries, universities and research institutes. Researchers struggle to access these funds efficiently. Competitive grants (e.g., via National Foundation for Science and Technology Development – NAFOSTED) are limited and spread too thin, and procedural hurdles delay disbursement. Moreover, public R&D is often not aligned to industry needs – firms report that university research rarely provides useful knowledge for them. In short, the public R&D apparatus is fragmented and heavily academic in nature, with limited focus on commercialization, yielding few patents or spin-offs relative to inputs (for example, tech-transfer revenue is under 1 percent of total revenue at major public universities). This inefficiency greatly dampens the innovation return on public investments.

Figure 26. Public and business expenditure on R&D

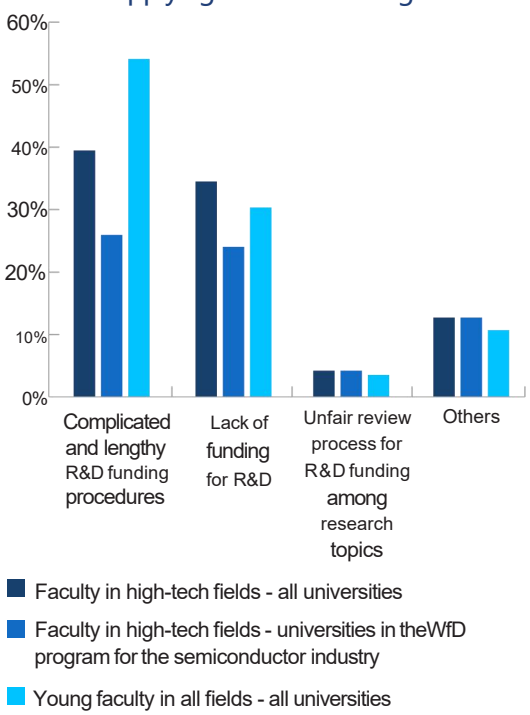


Sources: South Korea, the US, China, European Union, Singapore: OECD Main Science and Technology Indicators Database; Thailand: UNESCO Institute for Statistics (UIS), National Research Council of Thailand; Malaysia: UIS, Malaysia Science and Technology Information Centre (Ministry of Science, Technology and Innovation of Malaysia); Viet Nam: UIS, MOST of Viet Nam's 2024 report, Phillippines: UIS, Phillippines Congressional Policy and Budget Research Department Budget Brief 2022.

Note: Public expenditure on R&D (% of GDP) is calculated as the difference between total expenditure on R&D (% of GDP) and business expenditure on R&D (% of GDP). The proportion of Viet Nam's public expenditure on R&D total expenditure on R&D is collected from MOST (2024). Data for each country corresponds to the most recent year available.

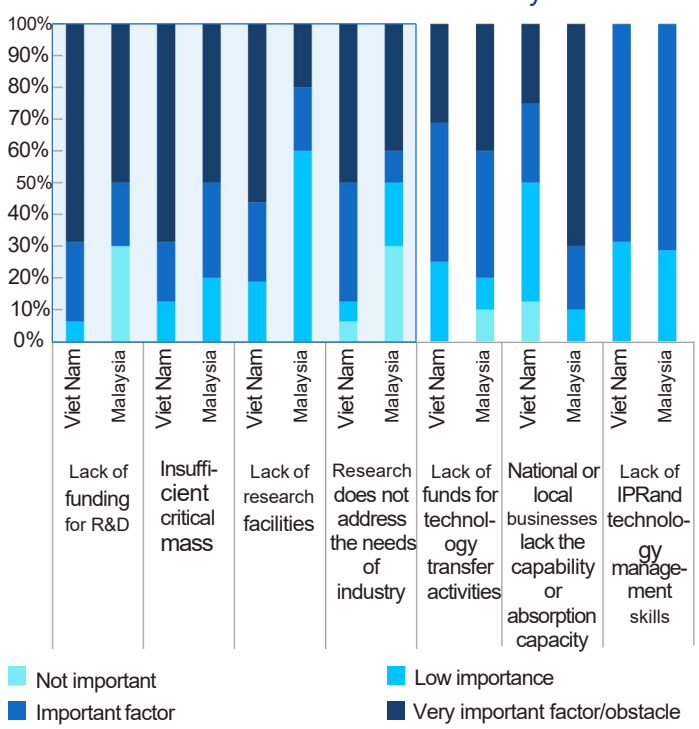
The key issues faced by all researchers in applying for research funding include low funding norms and standards, resulting in inadequately allocated research funding, and complicated and time-consuming funding application procedures before a funding proposal can be approved (Figure 27, Figure 28). In high-tech industries, researchers face similar challenges. However, for young researchers (having less than 5 years experience and aged under 36), complicated and time-consuming procedures present the biggest barrier.

Figure 27. Obstacles for researchers in applying for R&D funding



Source: World Bank staff calculations using the 2022 MOET-World Bank skills survey.

Figure 28. Obstacles to improving R&D outcomes for universities in Viet Nam and Malaysia



Source: World Bank. 2021. Cross-Country Survey on Research Funding Procedures. Washington DC.

3.6. Talent and innovation: implications for Viet Nam's value chain upgrading path

The findings of this assessment indicates that the lack of frontier talent and innovation capacity poses a fundamental constraint on Viet Nam's semiconductor value-chain upgrading. Viet Nam's higher education system has a strong foundation – large numbers of students interested in STEM, some well-regarded institutions and existing initiatives can be scaled, and the government is now prioritizing innovation – but it must overcome structural challenges to supply the talent needed for a semiconductor leap. This diagnostic also highlights areas requiring urgent action: boosting R&D spending (especially by firms), nurturing postgraduate education and research, and forging robust academia–industry linkages. Lacking this domestic innovation capital – talent and research – Viet Nam risks being confined to low-margin activities while competitors climb upwards.

Countries that successfully upgraded have all deliberately created a talent-R&D and innovation interlocking, supported by modernized infrastructure and ecosystem linkages. As discussed in Part II, SingaporeandChina are bothglobal and regional primeexamples.Theytightlycouple humancapitaldevelopment with R&D investment in a self-reinforcing cycle, despite different scales, policies and implementation. This twin strategy rapidly produced a "rich pool of highly skilled scientists" and world-class labs, leading to China's emergence as an innovation superpower in areas like AI, telecom, and new materials. This integrated approach – essentially linking talent supply, research, and industry – has enabled Singapore (despite its small size) to host cutting-edge semiconductor R&D centers and fabs.

For Viet Nam, the lesson is that ambitious talent development and innovation investments can yield quick gains - but only if pursued in tandem and at scale. Viet Nam's current siloed approach, higher education separate from research, and both distant from industry, must evolve in this direction to achieve a

similar upgrade. Programs to train or attract a critical mass of PhDs, coupled with well-funded centers of excellence in semiconductors, could similarly accelerate Viet Nam's move up-market. Conversely, without such efforts, policies to lure high-tech projects (fabs, design centers) may falter – companies go where the talent is.

There are no overnight fixes – they demand strategic, sustained reforms, and Part II of this report will therefore propose an integrated roadmap of policy measures – from scholarships and research funding to industry partnerships – aimed at building Viet Nam's own talent–innovation flywheel. The goal is to ensure the country not only has more engineers, but the right engineers and scientists to drive its semiconductor future.

PART II.

INTEGRATED INTERVENTIONS FOR THE GLOBAL SEMICONDUCTOR TALENT HUB AMBITION

This part envisions Viet Nam' s integrated higher education (HE) and innovation ecosystems that produce a high-quality workforce and drive innovation. In Part I, we established that while Viet Nam has strong ambitions and foundational strengths (a largeSTEM graduate pool, commitment from leadership), it faces interconnected, multidimensional challenges related to advanced skills, university capacity, and infrastructure. The proposed interventions address underlying structural constraints, while aligning with recent policy directives on breakthroughs in workforce, technology, and innovation.

Ultimately, companies gravitate to where cutting-edge talent and research converge - Viet Nam' s task is to cultivate that environment through sustained reforms and investment. China s and Singapore s cases, as mentioned earlier in Part I and illustrated in Box 1 and Box 3 below, underscore that significant progress is attainable with the right ingredients and long-term investment in talent and innovation. China s rise as an innovation and technology superpower shows that bridging human capital and R&D policy can yield dramatic gains: within a generation, China vaulted from low-end assembly to a global innovation leader, with firms and universities pushing technological frontiers. For decades, Singapore has treated workforce development and mission-oriented R&D as two interlocking gears of a single flywheel. While Viet Nam' s scale and context differ, embracing a similar talent-focused, globally engaged R&D strategy could markedly accelerate and sustain its journey up the semiconductor value chain.

The policy environment in Viet Nam as of 2025 is already markedly more enabling for HE and innovation reforms than ever before. The confluence of strong government commitment – through Resolution 57-NQ/ TW' s vision, the legal enablement via Resolution 193/QH15 and Decree 88/2025/NĐ-CP, and financial backing like the ISF creates a opportunity to leapfrog in innovation capacity. They altogether mark a shift toward a more integrated and mission-oriented development model. In summary, these instruments collectively: (a) set an ambitious strategic vision (57-NQ/TW) and action plan (03/NQ-CP) for STI-led development and digital transformation; (b) create legal frameworks to pilot new STI policies (193/QH15) and immediately implement them (88/2025/NĐ-CP) – fostering a more flexible, incentive-driven environment for research, HE, and innovation; and (c) introduce significant financing support to resource the effort, particularly in high-priority, strategic technology sectors (see the full policy landscape summary in Annex 6).

Part ll of the report identifies updated reform priorities and recommendations that build on what the Government has committed to do and suggests additional measures to ensure success. It lays out an integrated set of interventions, organized into four pillars:

(1) Ignite talent,

(2) Build shared R&D infrastructure,

(3) Catalyze university industry innovation, and

(4) Govern & finance for results.

Each pillar comprises specific actions for policy and investment, and the recommendations in this policy note reinforce the Government s intent by adding focus on implementation details: coordination, sequencing, and alignment with international best practices. They aim to accelerate delivery and reduce risks by ensuring that all parts of the ecosystem move in unison.

Underlying these proposals are the following principles and selection criteria:

- Close today' s gaps and pre-empt tomorrow' s: every action is chosen because it tackles the current skill shortages and the future gaps Viet Nam will face as it climbs the value chain.

- Build a full talent pipeline – stock and flow: measures strengthen the stock (existing scientists, engineers, technicians) while enlarging the flow of new graduates and upskilled workers needed each year.
- Act on three margins of scarcity: interventions boost the extensive margin (quantity of qualified talent), the intensive margin (depth of specialized, frontier knowledge and skills), and the integrative margins (training-to-work, lab-to-fab, R&D-integrated training).
- Sequence "quick wins" with long-term gains: early, visible results (e.g., bootcamps, shared EDA licenses) build momentum while laying foundations – cleanrooms, PhD pipelines – for the 2030 horizon.
- Augment, be adaptable, and scalable fora broader "Strategic Tech" agenda: the package is semiconductor-centric today, but every instrument can scale to other strategic technologies once scope and budgets are defined.

The overall objective is to ensure that HE institutions, research institutes, and industry can effectively collaborate and innovate, producing not only the skilled workforce and R&D outputs that Viet Nam's high-tech future requires, but ultimately also serving as a catalyst for creating high-quality, future-proof jobs that support sustainable economic growth. Annex 7 summarizes the underlying SWOT analysis of the intervention proposals in this report, laying out Viet Nam's internal strengths and weaknesses, as well as external opportunities and threats in developing a semiconductor talent ecosystem.

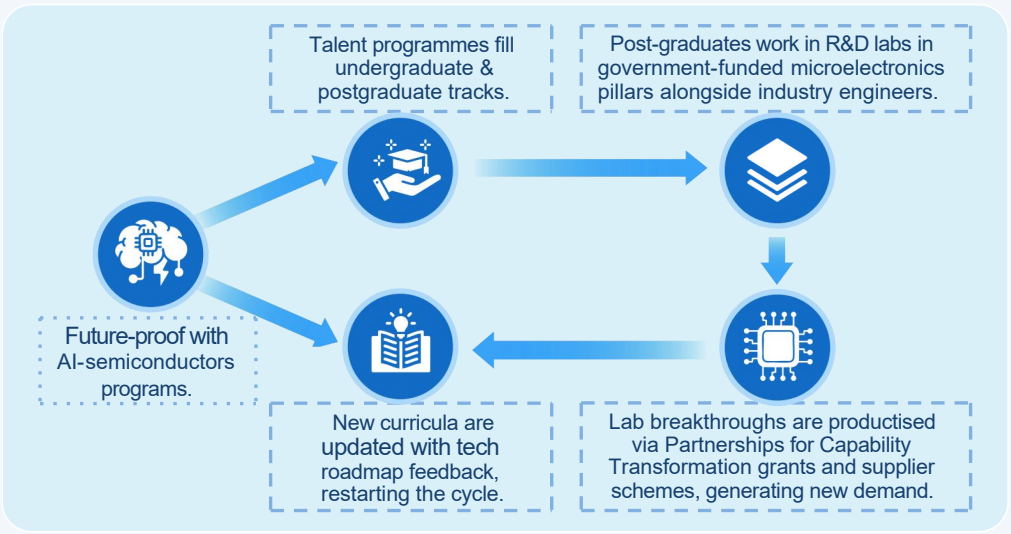
Table 8. Four intervention pillars and measures: Priority and feasibility

Intervention Pillar and Measures	Priority	Feasibility
PILLAR 1 – Ignite Talent – from classrooms to cleanrooms and design labs		
1. Semiconductor Fellowship Program for postgraduate training	S	High
2. Advanced upskilling and professional conversion	S	High
3. Faculty Excellence Fund / Program	S	Med
4. Semiconductor Fellowship for Faculty (nucleus leaders)	L	Med
5. Industry experience: internships, apprenticeships	S	High
6. Industry-linked curricula reforms	S	High
PILLAR 2 – Build Shared R&D Infrastructure		
7. National IC Design & Prototyping "Commons"	M	Med
8. University Lab Upgrade Program (both training & research)	S	High
9. Pilot Advanced Packaging & Testing Facility	M	Med
10. PPPs for high-impact, large-scale infrastructure	M & L	Low-Med
PILLAR 3 – Catalyse University–Industry–Government Innovation		
11. Matching-grant consortia for R&D	S	High
12. Technology Transfer Offices, Commercialisation funds & Startup vouchers	M	Med
13. "VITALS" program and pilot-line innovation hubs for academia-industry and FDI-local linkages and knowledge spillovers	M	High
PILLAR 4 – Govern & Finance for Results		
14. Semiconductor Talent Council (steering body)	S	High
15. One-stop financing platform	S	Med

Note: S – short term (2025-2026), M – medium term (2027-2030), L – long term (2031-2035)

Box 1. Singapore,s integrated semiconductor talent - innovation flywheel

Singapore treats workforce development and mission-oriented R&D as two inseparable gears of a single flywheel to drive the semiconductor industry and innovation.[33]



1. Talent pipeline: early attraction, deep skilling, continual conversion, together give firms confidence that specialized talent will be available at every technology node from production technicians to scientists.

- Early-stage exposure. The Singapore Industry Scholarship (SgIS) pays tuition and guarantees bonded employment, while an annual IC Design Summer Camp exposes Year 2+ students to design challenges.
- In-lab/fab Postgraduate. The Industry Postgraduate Programme (IPP) co-funds MSc/PhD candidates who spend half their time in company cleanrooms and labs.
- Technician ladder. All five polytechnics and the Institute of Technical Education co-design technician training pathways with firms, supplying skilled technicians for 24/7 fabs.
- Mid-career conversion. Career-Conversion programs, run jointly by the Singapore Semiconductor Industry Association (SSIA) and the Economic Development Board (EDB), retrain engineers from adjacent sectors.

2. Long-horizon, mission-oriented R&D funding with funding rules tied to talent development through the S$28 billion Research, Innovation, and Enterprise (RIE2025).[34] Four microelectronics pillars receive multi-year funding with projects receiving higher cost-sharing ratios when having Singapore-trained post-graduates. They are (1) heterogeneous integration & advanced packaging – facilities like the Applied Materials IME Center of Excellence and National University of Singapore s (NUS) SHINE "Chiplet" Centre host hybrid-bonding pilot lines for 2.5D/3D chip stacking; (2) Wide band-gap power semiconductors; (3) Sensors & actuators; and (4) Edge AI & photonics.

3. Ecosystem linkages for supplier depth and small and medium-sized enterprise (SME) spillovers. Singapore also co-funds industry partnerships to localize supply chains and foster innovation spillovers through the enhanced PACT.[35] The scheme supports five modalities of multinational corporation (MNC)-SME collaboration to keep know-how domestic and upgrade local firms alongside anchor fabs – supplier development, co-innovation, capability upgrading, internationalization, and corporate venturing. PACT grants ensure local SMEs capture advanced packaging and design know-how from MNCs, anchoring that knowledge in the domestic ecosystem.

Sources: WB staff compilation from various sources.

[33] Singapore Economic Development Board (EDB). 2024. What makes Singapore a prime location for semiconductor companies driving innovation? Singapore. Retrieved from https://www.edb.gov.sg/en/business-insights/insights/what-makes-singapore-a-prime-location-for-semiconductor-companies-driving-innovation.html

[34] Prime Minister' s Office (PMO). 2024. Remarks by Deputy Prime Minister Heng Swee Keat at the President' s Science & Technology Awards 2024. Singapore. Retrieved from https://www.pmo.gov.sg/Newsroom/DPM-Heng-Swee-Keat-at-PSTA-2024

[35] EDB. 2024. Enhanced Partnerships for Capability Transformation (PACT) Scheme Factsheet (COS 2024). Singapore.

1. IGNITE TALENT – FROM CLASSROOM TO CLEANROOM AND DESIGN LABS

This pillar focuses on developing the talent supply - both the stock and the flow - through education and training, as well as advanced upskilling (postgraduate training, credentials, etc.) – essentially, fast-tracking the quantity and quality of Vietnamese experts in semiconductors and related STEM fields. Financing will come from a mix of sources: primarily public (scholarships from the state budget), with contributions from industry (e.g., company-sponsored scholarships, paid internships).

Table 9. Ignite talent pillar: Three priority action areas and corresponding interventions

1. Advanced degrees & upskilling	1. Semiconductor Fellowship Program for postgraduate training 2. Targeted upskilling/ reskilling and professional conversion: semiconductor bootcamps, short cycle training, credentials, for engineers & technicians, within the semiconductor sector and from adjacent sectors (e.g., computer programming services, electronics manufacturing)
2. Faculty/ Research excellence	3. Faculty Excellence Fund/Program: faculty exchanges, visiting professors (to Viet Nam), co-sponsoring postdocs, funding and secured research grant and position upon returns, faculty/professor of practice 4. Semiconductor Fellowship Program for faculty for nucleus faculty/ research leads
3. Industry linkages	5. Industry experience: internship, apprenticeship 6. Industry-linked curriculum renovation

1.1. Scale up advanced degrees and upskilling

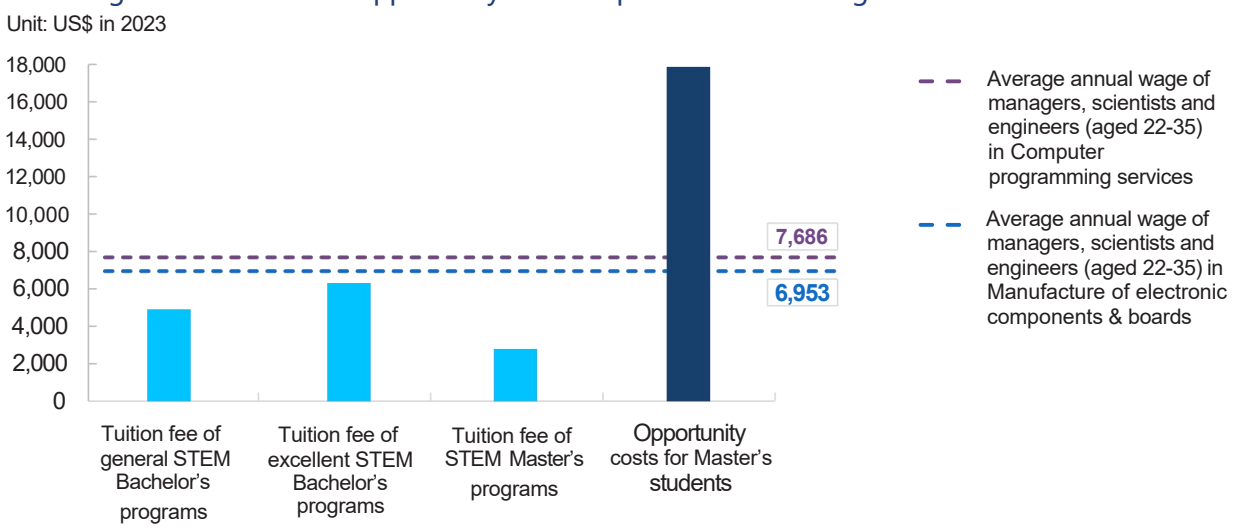
The first and top priority is to invest in postgraduate education and other advanced professional short-term training programs. The lack of postgraduate-level talent is a binding constraint for the scale and quality of training through the faculty pipeline, scaling up R&D and design activities, and ensuring the retention of top talent for the whole ecosystem. This is valid not only for semiconductors but also for other high-tech industries.

Postgraduate fellowship and twinning programs

A Semiconductor Fellowship Program could provide scholarships, stipends, or tuition waivers for at least 500 Master's and PhD students in critical STEM fields per year over the next 5-7 years. The incentives and level of support must approach market offers and be able to offset the opportunity costs of pursuing postgraduate training (Figure 29). The program can be modeled after South Korea's Brain Korea 21 (BK21) or Taiwan (China)'s government scholarships, which helped produce an R&D workforce for those countries. Selection should target fields critical to the semiconductor chain (microelectronics, nanomaterials, computer engineering, etc.) and include a mix of domestic and overseas graduate study, with clearly defined bonding agreements to return. The aim is that by 2030, Viet Nam at least doubles or triples the annual output of Master's/PhDs in these fields.

In parallel, domestic Master's and PhD programs could be strengthened by twinning Vietnamese universities with top foreign programs. Leading technical universities in Viet Nam have already partnered with – and could further strengthen their bonds with foreign universities to co-design and offer joint Master's and PhD programs in Semiconductor Engineering and other related fields. PhD students can be co-supervised by faculty from both Viet Nam and the foreign universities. This approach will ensure that curriculum and research meet global standards. The government can fund faculty exchanges and visiting professors to support these joint programs, as discussed in the next section.

Figure 29. Tuition and opportunity costs for potential Master degree students in Viet Nam



Sources: World Bank staff calculations based on universities' disclosed tuition fees, LFS 2023.

Notes: Tuition fee is for the whole program. Bachelor's programs typically last 4-5 years, Master's programs generally span 1.5-2 years. Opportunity costs for Master's students during the training time equal the average tuition fee of STEM Master's programs plus the average annual wage of young university-educated workers in Computer programming services and Manufacture of electronic components & boards.

The anchor universities in Viet Nam hosting these postgraduate programs could pursue a hybrid model, which balances central coordination (centralized) and departmental autonomy (decentralized). This model requires a well-resourced centralized Office of Postgraduate Education, led by a dedicated dean, to oversee university-wide postgraduate policies, quality assurance, admissions standards, and funding mechanisms (for students). Individual academic departments would be responsible for the design and delivery of their specific graduate programs, managing curriculum development, faculty supervision of students, and coordination of lab work within the university-wide guidelines. Both the centralized office and the departments should work closely with the career office, industry partners, and the government to support job placement opportunities for graduates from the Fellowship program.

Advanced upskilling and professional conversion

Given fast-evolving skill requirements and technology changes, it is imperative to establish a continuous advanced upskilling model and professional conversion for Viet Nam's existing semiconductor workforce and those from related sectors. These workforce development schemes are key to fostering a lifelong learning culture in a rapidly evolving technology landscape.

Viet Nam is already making progress in these areas. TheNIC, under the Ministry of Finance (MOF), has launched a Semiconductor Training and Incubation Program in collaboration with U.S. industry partners. For example, in July 2024, NIC partnered with Qorvo and Cadence to initiate training programs aimed at contributing to the target of 50,000 semiconductor engineers by 2030.[36] Courses on analog IC design have commenced, with industry experts directly teaching Vietnamese students. In mid-2025, Lam Research, a leading U.S. semiconductor equipment firm, committed to supporting Vietnam's semiconductor workforce by providing state-of-the-art training equipment and technologies to selected Vietnamese universities.[37] Additionally, major universities like VNUHCM have signed agreements with companies such as Marvell and Synopsys to incorporate chip design into their curricula, with the goal of training thousands of engineers and hundreds of Master's students in IC design.

[36] DIGITIMES Asia. (2024, July 25). Vietnam's NIC launches analog IC course with Cadence, Qorvo to reach 50,000 engineers goal. Retrieved from https://www.digitimes.com/news/a20240725VL200/vietnam-nic-analog-ic-training.html

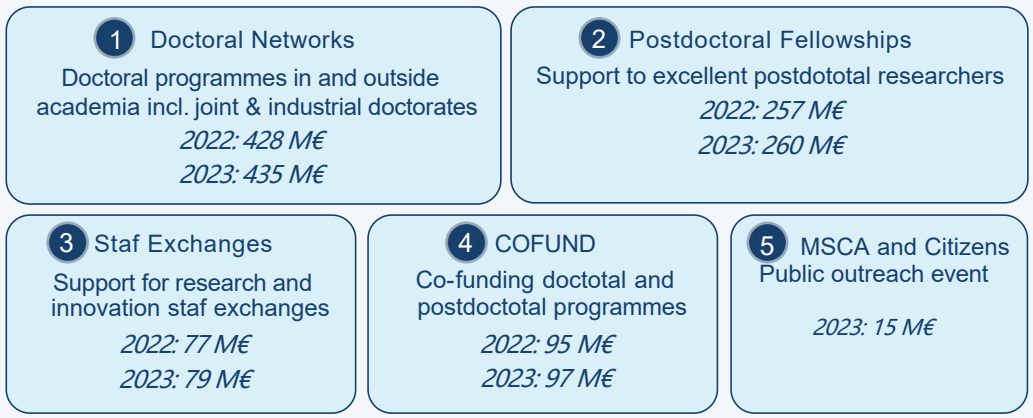
[37] VietnamNet. (2024, March 30). US giant funds semiconductor training tech for Vietnam. Retrieved from https://vietnamnet.vn/en/us-giant-funds-semiconductor-training-tech-for-vietnam-2411025.html

Box 2. Global parallel - University-industry co-create and co-delivery of postgraduate programs

1. Taiwan' s TSMC Graduate Program – In Taiwan (China), TSMC has a long-standing partnership with local universities, funding specialized graduate institutes in semiconductor disciplines.[38] TSMC co-designs the curriculum and offers students hands-on projects. Many Master' s/PhD students have TSMC supervisors alongside their professors, and they typically join TSMC upon graduation. This model ensures a tight academia–industry linkage and a steady supply of highly trained talent for the company. Viet Nam can emulate elements of this by engaging big employers (like Samsung, Intel) to co-sponsor scholarships or thesis projects. It essentially functions as a pipeline, with industry actively involved in training its future workforce during their graduate studies.

2. Europe' s Marie Skłodowska-Curie Actions (MSCA) [39]– The MSCA (details in the figure below) are the EU' s flagship competitive grant programs for strengthening the research workforce by encouraging young people to pursue research careers, attracting and retaining top researchers, and reintegrating diasporans. Grants are co-funded by the EU and the participating universities or consortia of universities and other institutions.

   Industrial Doctorates is a doctoral program funded by the MSCAto promote academic–industrial partnerships. Doctoral candidates are jointly supervised by academic and non-academic partners and must spend at least 50 percent of their research time at non-academic institutions. Funding ceilings (in the form of the number of funded PhD candidates per consortium) are higher for Industrial Doctorates than for standard Doctoral Networks, further encouraging large-scale collaboration.



Sources: WB staff compilation from various sources.

However, more structural and sustainable progress is needed. This report proposes a three-tier upskilling framework that could be co-led by industry and select anchor universities (semiconductor education hubs): (i) intensive bootcamps for mid-career engineers, (ii) vendor-led academies, and (iii) professional conversion programs.

First, short-term training and certification programs, such as micro-credentials, including stackable modules that could lead to a degree), can target existing engineers and technicians from the semiconductor industry and adjacent sectors (e.g., electronics manufacturing, IT services), training them in semiconductor-specific skills (e.g., IC design fundamentals, packaging process engineering). The NIC and leading universities may offer annual semiconductor bootcamps – 3–6-month intensive courses in areas like

[38] Taiwan Semiconductor Manufacturing Company (TSMC). n.d. TSMC University Collaboration Programs: ESG Case Study. Retrieved from https://esg.tsmc.com/csr/en/update/innovationAndService/caseStudy/2/index.html; Taiwan Semiconductor Manufacturing Company (TSMC). 2021. TSMC Ph.D. Scholarship Program to Cultivate High-Level Talent: ESG Case Study. Retrieved from https://esg.tsmc.com/en/update/innovationAndService/caseStudy/38/index.html

[39] European Commission. 2021. Marie Skłodowska-Curie Actions 2021-2027 – Factsheet. Brussels. Retrieved from https://marie-sklodowska-curie-actions.ec.europa.eu/sites/default/files/2021-06/MSCA_2021_27-factsheet_FINAL.pdf

IC design, verification, or semiconductor processing. Industry experts can serve as co-designers and co-instructors, and participants could include new graduates or mid-career engineers from related fields (e.g., electrical engineering, mechatronics) who wish to transition to semiconductors, as well as those already in the semiconductor industry who require upskilling. The government can provide vouchers to subsidize trainees, particularly targeting underrepresented groups (such as women in engineering). The expected annual output is a few hundred certified specialists ready to transfer to the semiconductor industry. Industry partners could also provide financial incentives for their employees to benefit from these reskilling and upskilling opportunities.

Second, major semiconductor investors should be encouraged to establish vendor academies in Viet Nam. Firms like Intel and Amkor already operate extensive in-house training programs for their staff. Opening up portions of these programs or setting up joint academies for the broader talent pool would greatly expand practical skills training. Formal vendor academies could offer certified courses on topics such as advanced lithography, test engineering, or analog IC design, using curricula co-developed by the companies. These academies would not only produce job-ready technicians and engineers but also ensure that training content stays current with technology trends, as industry would drive the training.

Third, Professional Conversion Programs (PCPs) - inspired by Singapore's PCP - can facilitate mid-career transitions into semiconductors. Singapore's experience demonstrates that conversion schemes integrating targeted training with job placement can effectively channel experienced professionals into new high-tech roles. For example, a Vietnamese PCP could recruit mid-career electrical or automation engineers from adjacent industries (e.g., electronics, electrical equipment) and reskill them as semiconductor process or equipment engineers through a 6-month blended classroom and customized on-the-job training program (e.g., apprenticeships). Government support would help trainees during training and role transitions while also reducing barriers for firms to hire these trainees.

Central to this intervention is an MNC-led co-funding approach with strong government incentives. Upskilling at scale is resource-intensive, and costs should be jointly borne by the public and private sectors. These FDI firms – who directly benefit from Viet Nam's enlarged skilled workforce – are expected to contribute at least 50 percent. In practice, this means companies co-financing bootcamp cohorts, contributing trainers to vendor academies, and co-sponsoring conversion programs, possibly in return for hiring commitments. Such public private partnerships for workforce development are already being discussed in Viet Nam s policy circles. High-tech firms will be reimbursed for 50 percent of the cost of on-the-job skills upgrading, with funding from the ISF (Decree 182/2024/NĐ-CP). By requiring greater industry commitment, programs will become more demand-driven and sustainable.

1.2. Attract and cultivate excellent faculty and researchers

With the gaps and bottlenecks discussed in Part I, Viet Nam needs more qualified training and research faculty in universities and research institutes. The proposals below aim to support this area.

A Faculty Excellence Funding Window/Program (FEF) could play a pivotal role in upgrading faculty capacity in semiconductor-related fields. This program would serve multiple purposes: sending young lecturers abroad for PhDs (with full funding, an obligation to return, and an early-career research grant upon return); co-sponsoring postdoctoral fellowships for Vietnamese scholars in top overseas labs; and bringing foreign or diaspora experts to Vietnamese campuses as visiting professors. For example, 50 promising young Vietnamese lecturers could be identified across universities and fully sponsored to pursue PhDs in countries such as the US, China, Taiwan (China), or Europe in semiconductor disciplines. Upon completion, they would receive a research grant and a secured faculty position back home.

The funding window could also provide performance incentives for existing faculty and attract visiting faculty from industry. For current faculty, incentives might include additional funding to establish new courses or labs in semiconductor fields, or extra support for publishing research in high-impact international peer-reviewed journals (drawing lessons from VUDP). Other incentives may include support for research commercialization or matching grants for faculty who secure external funding from international competitive grants or industry-sponsored projects. This initiative could also include a program for faculty sabbaticals in industry. For example, universities could allow and encourage professors to spend 6–12 months working at a semiconductor company (domestic or international), while experienced industry professionals could be brought into universities to teach or mentor students. A professor undertaking a sabbatical in industry could have their university salary supplemented by the company or through a government stipend.

For potential industry experts entering academia, Decree 88 offers flexibility to address traditional bureaucratic barriers. A retired engineer from TSMC or an expert from imec could be invited to teach a semester in Viet Nam under attractive terms. Singapore has implemented similar initiatives through its Global Visiting Professorship programs. For both existing faculty and incoming industry professionals, the combination of these incentives should match or at least approximate the market offers available to similarly qualified talent. This kind of cross-pollination helps ensure that curricula remain current and that research maintains practical relevance.

A "Semiconductor Nucleus Fellowship for Faculty" initiative could be established within the proposed Faculty Excellence Funding Window. This initiative would competitively select a cohort of faculty in Viet Nam's universities and provide them with targeted grants (for equipment, PhD student support, etc.) to become nucleus leaders in specialized subfields such as analog design, power electronics, or micro-electro-mechanical systems (MEMS). This could be modeled after South Korea's BK21+, which funded university research groups and tracked outcomes. South Korea's experienced significant increases in both research publications and technology commercialization from these groups – a success from which Viet Nam can draw important lessons.

Finally, leveraging the Vietnamese diaspora is critical. Many Vietnamese engineers and researchers in Silicon Valley, Taiwan (China), and other regions have expressed interest in contributing. This dedicated faculty funding window could support visiting programs, enabling diasporans to teach specialized short-term courses (e.g., summer programs) or contribute as research advisors. Many would be willing to participate if expenses are covered and their efforts are formally recognized. Such engagements not only facilitate knowledge transfer but also help catalyze long-term partnerships. A focused network for semiconductors could be established with partial funding and strong government backing.

1.3. Modernize curricula by deepening industry engagement

Curricula modernization is key: a consortium of leading technical universities, in partnership with MOET and the Ministry of Science and Technology (MOST), should fast-track new curriculum standards for semiconductor-related programs while maintaining international quality standards. This means that by 2025, a working group should be commissioned, consisting of relevant faculty from local universities, an Academic Advisory Board, and a Semiconductor Industry Advisory Board to co-create reference curricula for undergraduate, Master's, and PhD tracks (e.g., VLSI design, chip fabrication). These boards (with members from companies like Intel, Amkor, Viettel, FPT, etc.) should meet at least twice a year for subsequent review of course content, suggest updates (such as adding a course on AI hardware design or on supply chain for fab management), and facilitate activities such as guest lecture series, equipment donations, and coordination of experiential learning opportunities for students. South Korea's Innovation Sharing University program provides a model, where multiple universities share courses and involve industry consortiums to develop content. In Viet Nam, VNUHCM, VNUHN, and HUST have embraced a similar pathway and recently joined hands in co-creating and delivering training and research in strategic areas.

Box 3. China's tech talent and emergence as a global innovation superpower

China's experience over the past two decades demonstrates how a country can rapidly ascend the technology ladder by synchronizing investments in talent and R&D at scale. China built a self-reinforcing innovation ecosystem by making large-scale investments in R&D and workforce development, particularly in strategic fields such as electronics, advanced materials, and AI. These investments improved laboratories and research opportunities, attracted home large cohorts of Chinese STEM talent trained in the US and Europe, and cultivated domestic expertise. Returnees – supported by generous grants, cutting–edge facilities, and strong career prospects – helped generate intellectual property and high-tech firms, further fueling the innovation cycle.

From 2000 to 2018, the number of STEM PhD students in China increased more than fourfold. During this period, STEM consistently accounted for the majority of doctoral students graduating from Chinese universities. In 2000, the number of PhD graduates from Chinese universities was less than one-third of the number in U.S. universities. However, by 2018, China had nearly caught up with its U.S. counterparts. Following the same trend, China's annual number of STEM PhD graduates is expected to almost double that of the US by 2025.

Approximately 45 percent of Chinese doctoral graduates come from "Double First Class" (DFC) universities, which represent the top-tier institutions in China. DFC universities are those included in the Double First Class University Initiative – a continuation and refinement of government policies focused on building world-class universities in China. These institutions have received substantial central government funding for education and research to achieve this goal. As of 2024, the Double First-Class initiative includes 147 universities, four of these institutions rank in the global top 50 (Tsinghua, Peking, Fudan, Zhejiang), seven in top 100, 13 appear in the top 200, and roughly 36 – about one in four – are positioned in the top 500 worldwide.

This combination of generous resources, sustained human capital development, and global collaboration has propelled Chinese innovation outputs and quality to the global frontier. Perhaps most strikingly, in a number of frontier technology domains – ranging from 5G telecommunications to battery chemistry, artificial intelligence, and advanced materials – the quality of China's research and patents is now approaching the global frontier. China, for two consecutive years in 2023 and 2024, leads with the most science and technology clusters (26) in the global top 100.

Sources: WB staff compilation from various sources – China MOE 2022; CSET, 2021; CSIS, 2024; NSB, 2024; WIPO, 2024.

Ensuring that students - especially those in the design track - have access to modern EDA tools and prototyping labs will immediately raise the quality of training and research projects. As elaborated in the next pillar on Infrastructure, the government could fund an EDA "commons" with centralized negotiations, where universities can access industry-standard design tools and prototyping resources. Likewise, shared access to specialized laboratory facilities, as part of the IC Design & Prototyping "Commons" in the Pillar 2 on Infrastructure, should be provided so that students can practice on modern fabrication, testing, and packaging equipment. For example, integrating vendor certification modules (Cadence, Synopsys, etc.) into coursework can allow students to graduate with industry-recognized tool certifications. Investing in such a "commons" addresses today's fragmented university–industry linkages – to date, only isolated donations of software or equipment have occurred – by systematizing academia's access to cutting-edge technology. Additionally, industry certifications should be integrated into curricula, so students graduate not just with a degree but also with tool certifications valued by employers.

Internship, project-based learning, and industry exposure must also be a cornerstone of university training programs. Every semiconductor engineering student should complete an internship or industry project before graduation. Work-integrated learning should be ubiquitous in the curricula – whether through cooperative education (alternating study and work semesters), internships, or a capstone project mentored by engineers. The government can incentivize companies to host students by subsidizing stipends for students via the ISF (workforce training window). Over time, this practical training will improve employability and ensure

graduates have hands-on experience with tools and real-world problems. (MNC-to-local skills spillovers are addressed through the VITALS proposal under Pillar 3.)

Taken together, the Talent interventions aim to close today's critical skills gaps while also building the advanced competencies needed for tomorrow's semiconductor industry. They boost the extensive margin of talent (training more engineers and researchers), the intensive margin (deeper specialized skills per person), and the integrative margin (training-to-work, research-integrated training, conversion), co-designed and co-delivered with the industry. Crucially, these measures also lay the groundwork for Viet Nam's move up the value chain: a larger pool of postgraduates and industry-savvy graduates will support more design and R&D activities domestically, and stronger faculty and curricula will produce the innovators and entrepreneurs of the next decade. The parallel effort must be to provide these talented people with the facilities and incentives to innovate at home – which the next pillars address.

2. BUILD SHARED TRAINING AND R&D INFRASTRUCTURE

The second pillar addresses the hardware side of the talent equation: the facilities and equipment needed for training and research. The strategy is to invest in university foundational training and research infrastructure and leverage shared R&D infrastructure so that Viet Nam s talent and industry have access to world-class labs without each actor bearing the full cost. By pooling resources, Viet Nam can overcome the capital intensity barrier and accelerate innovation.

2.1. Establish an lC Design & prototyping "Commons"

Viet Nam' s talent development will benefit from creating a national lC Design Center (a "Design Commons") that serves as a hub for semiconductor design activities open to universities, startups, and even established firms. This center could be part of a larger national semiconductor/high-tech hub and facilitate access to:

- digital infrastructure, such as high-performance computing resources for chip simulations and AI/ML research, cloud storage, and data centers in close collaboration with VinaREN;
- a central library of EDA tools (with enough licenses for many users); and
- a repository of common IP cores that designers can use.

The center could also facilitate multi-project wafer (MPW) shuttles where multiple prototype chip designs from different teams are fabricated simultaneously on a single wafer, enabling teams to share the cost of fabrication runs (as is commonly done via services like the Metal Oxide Semiconductor Implementation Service (MOSIS) in the US). The goal is to lower the barriers for a student, faculty group, or startup to design, fabricate, and test a chip. VNUHCM, VNUHN, and NIC-HUST could host this center at the national semiconductor hubs to be established.

By having a central facility, Viet Nam could negotiate better deals on tools and short-run fabrication, and ensure that everyone from students to small startups can go from concept to chip prototype with minimal upfront investment. This directly supports upskillings, students, upskilled workers, and faculty, gain hands-on experience with actual chip tape-outs, and spurs innovation (making it easier to experiment with new designs).

2.2. Launch a "University Lab Upgrade" program with operation and maintenance

Broad-based capacity development and key universities could benefit from a system-level grant program to upgrade foundational and advanced training laboratories. For example, 5 10 universities, in addition to those who will lead the national hubs, could also be selected to receive grants on a competitive basis (e.g., US$5 10 million each) to bring their electronics and materials labs up to modern standards (equipment for nano-fabrication, characterization, etc.). However, to avoid the common pitfall of equipment lying unused, each grant should include a portion dedicated to training lab technicians and maintaining equipment. To ensure sustainability and maximize utilization, universities should be required to have maintenance contracts for critical machines and to share usage within the university (if under the VNU and/or regional university umbrellas) and with other institutions via an online booking system coordinated by a lead agency.

Joint industry-university labs and centers of excellence: Thematic Centers of Excellence (CoEs) within universities could be co-funded by industry. Already, some Vietnamese universities have labs sponsored by

companies (e.g., the Marvell Lab at HCMUT, a software lab by FPT at UIT, the Viettel-HUST 5G/6G Lab at HUST).[40] [41] The goal is to scale up this concept to more strategic labs. For instance, a "Center for Analog IC Design" at HUST could be initially funded by a government grant, but required to secure industry-sponsored projects to sustain operations after several years. These centers would bring together faculty and students across departments to focus on strategic industries (e.g., high-tech) and collaborate with industry. The priority theme could cut across sectors. The CoEs could even be set up as semi-autonomous entities (with their own governance structure that includes industry representatives). If successful, they could later be spun off as specialized institutes or even companies.

The overall long-term sustainability of these CoEs should be built into their design. CoEs generally require sustained public funding for at least 10 15 years, followed by a gradual transition toward increased industry co-funding in subsequent phases. This minimum 10 years ceiling for public funding is applicable even in mature innovation ecosystems as the US (Rand Corporation, 2024; NSF, 2025). Similar to the training labs, and to ensure sustainability and maximize utilization of specialized equipment, each grant would include dedicated funding for lab technicians and equipment maintenance. However, each CoE would also be required to have a maintenance plan, which could include maintenance contracts with equipment vendors and a fee model for the use of its specialized equipment. A centralized online booking system, managed by a lead agency, would enable coordinated access to labs among CoEs, academic institutions, and industry users.

2.3. Pilot an Advanced Packaging and testing facility

Given Viet Nam' s existing strength in assembly and test, a logical next step is to create a shared advanced packaging R&D line if the country moves into advanced packaging. Essentially, this is a pilot manufacturing line where new packaging technologies and materials can be tested, and where workforce training and research can occur on real equipment. This would require establishing an Advanced Packaging Tech Center, in collaboration with industry. The facility would be equipped with the latest packaging tools (e.g., for 2.5D interposers, flip-chip bonding, and even exploratory technologies like silicon photonics integration). Companies such as Amkor or even Samsung might partner, bringing in equipment and experts, while the government co-funds the capital and operational costs.

Researchers and students could use the facility for research and academic projects (under appropriate IP agreements), and companies could prototype new packaging solutions without disrupting their mass production lines. Japan s model of consortium labs (e.g., the planned Leading-edge Semiconductor Technology Center LSTC) and Belgium s imec both demonstrate that having a neutral R&D fab operated on a non-commercial and non-exclusive basis – benefits the entire ecosystem (see Box 4).[42] [43] Viet Nam should fast-track the feasibility study for such a center by 2026, potentially hosted at one of the national semiconductor hubs mentioned earlier.

2.4. Public-Private Partnerships (PPPs) for high-impact, large-scale infrastructure

Some infrastructure, like a full-scale national semiconductor hub, is beyond the scope of government-alone funding, and PPPs can make it happen. Table 10 and Box 4 provide examples from Singapore, Japan, and Belgium, on how the government, academia, and industry join forces for large-scale semiconductor infrastructure. In the case of Viet Nam, the government could approach a memory chip packaging firm or a fabless company to establish an R&D center in Viet Nam, offering the incentive that the government (via the

40 Ho Chi Minh City University of Technology. (2025, April 3). Semiconductor lab and resources funded by Marvell soon to be operated. Retrieved from https://oisp.hcmut.edu.vn/en/news/semiconductor-lab-and-resources-funded-by-marvell-soon-to-be-operated.html

41 Hanoi University of Science and Technology. (2024, December 27). Inauguration Ceremony of the Viettel-HUST 5G/6G Lab. Retrieved from https://hust.edu.vn/en/news/news/inauguration-ceremony-of-the-viettel-hust-5g-6g-lab-653984.html

42 LSTC. (2022, December 21). Japan to establish Leading-edge Semiconductor Technology Center (LSTC). Retrieved from https://www.meti.go.jp/english/press/2022/1221_001.html

43 Imec. (n.d.). Imec: Advancing semiconductor innovation with global partners. Retrieved from https://www.imec-int.com/en/about-imec

Investment Fund) will cover 50% of the setup cost and provide tax incentives. In return, the investor would be required to link with local universities (e.g., workforce upskilling, training programs, and allowing faculty to conduct research at the facility). Another example could involve the government inviting a global OSAT firm to build an R&D site focused on advanced testing, with the state budget covering half of the construction cost. The site could partner with universities such as the VNUs or HUST to deliver training programs.

It is important that for large infrastructure investments, the government earmarks approximately 10-15 percent of the capital cost as a maintenance endowment, whose returns fund upkeep and periodic upgrades. Alternatively, the government could negotiate with equipment vendors to include multi-year servicing in procurement contracts (especially for equipment such as electron microscopes or etchers). For example, when purchasing a US$5 million tool, a clause could be included requiring the vendor to provide maintenance support and training for five years as part of the deal. This practice is common in high-end lab procurements globally imec, for example, ensures that companies involved help maintain the equipment.[44]

Table 10. Singapore's investment in high-impact infrastructure for semiconductor innovation

Pillar	Programme / Facility	2024-25 Highlights & Strategic Value
1. Heterogeneous-Integration Centres of Excellence[45]	Applied Materials A*STAR Advanced-Packaging CoE (Science Park II) & EPIC Advanced-Packaging Platform	• Joint lab (since 2011, 170+ R&D staff) now anchors Singapore s hybrid-bonding "lab-to-fab" line; a partnership between 05 A*STAR's research institute, allowing partner companies to tap the tool sets for 2.5D/3D chip stacking and power-efficient AI accelerators.
	NUS SHINE "Chiplet" Centre	• A national heterogeneous-integration pilot line; co-locates university researchers with specialty foundries, offering "mix-and-match" chiplet packaging for IoT and edge-AI markets.
2. Wide-Band-Gap (WBG) Pilot Lines[46]	IME 200 mm SiC Open R&D Line	• World's first open 200 mm SiC pilot line (December 2023) partners with Centrotherm
	National GaN Technology Centre (NGTC)	• Translational hub run by A*STAR, Nanyang Technological University (NTU) & DSO with small-volume manufacturing for industry pilots.
3. Prototype-to-Production Bridge[47]	National Semiconductor Translation & Innovation Centre (NSTIC)	• US$132 mil. RIE2025 flagship (opened April 2024) offers shared clean-room, scientists & IP pool for silicon-photonics & flat-optics prototyping and small-lot runs.
	NSTIC (R&D Fab) Expansion	• New 15 000 m² fab at JTC nanoSpace@Tampines (operational 2027) gives start-ups access to industry-grade tools, closing the scale-up gap.
4. Supply Chain: SME and Upskilling[48]	PACT Grant Scheme	• Defrays manpower, equipment and software costs for MNC SME partnerships across supplier-development, co-innovation and capability-training; five modalities cover the full electronics chain.

44 Imec. (n.d.). Supplier Manual. Retrieved from https://www.imec-int.com/sites/default/files/inline-files/Supplier%20Manual%20imec.pdf; Imec. (n.d.). General Purchasing Conditions. Retrieved from https://www.imec-int.com/sites/default/files/inline-files/general-terms-and-conditions-purchase.pdf

45 Ministry of Trade and Industry Singapore. (2024, November). Speech by DPM and Minister for Trade and Industry Gan Kim Yong atthe Launch of Applied Materials Future Fab Singapore. Retrieved from https://www.mti.gov.sg/Newsroom/Speeches/2024/11/Speech-by-DPM-and-Minister-for-Trade-and-Industry-Gan-Kim-Yong-at-the-Launch-of-Applied-Materials; ASTAR. (2024, November 21). ASTAR and Applied Materials establish joint lab to accelerate semiconductor innovation in Singapore. Retrieved from https://www.a-star.edu.sg/News/astarNews/news/press-releases/astar-applied-materials-joint-lab-semiconductor-innovation-singapore; National University of Singapore. (n.d.). Semiconductors HorizonNUS Interdisciplinary Enterprise (SHINE).

46 ASTAR. (2023, October 25). ASTAR and Centrotherm establish partnership to advance 200mm silicon carbide technology. A*STAR Institute of Microelectronics. (n.d.). mmWave GaN Technology. Retrieved from https://www.a-star.edu.sg/ime/Research/mmwave-GaN

47 Singapore Economic Development Board. (2024, April 24). Singapore semiconductor companies, including startups, can tap new S$500 million National Fab Facility by 2027.

48 Singapore Economic Development Board. (n.d.). Partnerships for Capability Transformation (PACT) Scheme. Retrieved from https://www.edb.gov.sg/en/grants/incentives-and-schemes/partnerships-for-capability-transformation-pact-scheme.html

Box 4. Global parallel – PPP for high-scale, large impact infrastructure

imec

- imec (Belgium) is a world-renowned nanoelectronics R&D hub that has a unique cost-sharing model.
- imec' s key feature is a consortium governance: initial funding comes from government and donors, and firms contribute via membership or project fees, ensuring that the consortium could be self-sustaining over time.
- The imec model has been referenced in internal discussions for Viet Nam as a template.

INDUSTRY MEMBERSHIP MODEL

- Industry partners pay an annual membership fee and provide resources
- imec offers design, prototyping, testing, consulting, fab services
- Companies collaborate with each other

CONSORTIUM GOVERNANCE

1984: 100% govt investment
1990s: 50% govt investment
2023: 25% govt investment

- Convening agency with operational autonomy
- Hundreds of PhD candidates do research at **imec**

LSTC 技術研究組合 最先端半導体技術センター Leading-edge Semiconductor Technology Center

- LSTC (Japan) aims to advance next-gen 2nm process technology.
- LSTC is a research lab shared among tech companies, universities, and the government, with each contributing funds and expertise to operate it.

INFRASTRUCTURE PPP

- Shared research fab, aim for cutting-edge 2nm technology
- Industry, universities, and government each contribute funds and expertise, sharing the cost burden

3. CATALYZE UNIVERSITY-INDUSTRY-GOVERNMENT INNOVATION

Viet Nam's semiconductors ambition to cIimb towards higher vaIue-added' R&D-intensive segments wiII faIter without a steep change in the integration of academia and industry in innovation. Currently, collaboration is limited and ad hoc: few joint labs or co-funded projects exist, and technology transfer from universities is minimal (over 85 percent of tech-transfer contract value in recent years came via foreign firms, not local universities). This pillar aims to catalyze a virtuous cycle of innovation whereby universities become engines of semiconductor technology (rather than ivory towers), and firms actively draw on local research and talent. The recommendations focus on incentives and platforms that blend the two worlds, ensuring that knowledge flows freely from lab to market – and back again.

3.1. Matching grants for joint R&D consortia

Competitive grant programs for semiconductor R&D that require university-industry coIIaboration couId spur innovation between the two sectors. Currently, the government is providing matching grants for R&D projects, in which government grants account for 30–50 percent of project costs, but these programs are few and fragmented. A Semiconductor Innovation Challenge Window, housed within one of the priority innovation funds for strategic industries and high technologies, could be established. Under this scheme, consortia comprising at least one university and one company would apply for funding for joint R&D projects. The grants would be matching – for example, the government would provide 50 percent of the project cost, and the industry partner would provide the remaining 50 percent (in cash or in-kind). Such matching grants encourage both sides to commit resources and focus on applied outcomes. This ensures that both sides have skin in the game and that projects are oriented toward practical, real-world impact.

ln 2025-2026' Viet Nam couId piIot the scheme with a modest budget (e.g.' a few miIIion US$) to test demand and refine implementation processes, then scale up if successful. Proposal selection criteria should include commercial relevance (a clear use case or market need) and talent development (e.g., involvement of graduate students or inclusion of training components). Countries like Malaysia and Singapore have used similar matching R&D grants to great effect – they stimulate applied research, forge lasting partnerships, and ensure that academic R&D addresses real industry problems rather than remaining siloed. The program could be administered by a national STI funding agency, with open calls for proposals and an evaluation panel including international experts and industry veterans to ensure quality and relevance.

3.2. Technology transfer offices, entrepreneurship-in-training, and startup vouchers

Technology transfer

TechnoIogy Transfer Offices at major universities shouId be strengthened' potentiaIIy by pooIing resources across institutions (e.g.' one office serving a network of universities). Training on IP management and seed funding should be provided to these offices. More importantly, the government could consider establishing a grant program to support deep tech proof-of-concept activities, especially in semiconductors. For example, if a research group develops a novel sensor, a grant could fund the development of a prototype or support market validation efforts.

A cuIture of spinning off companies or Iicensing technoIogy shouId aIso be cuItivated. South Korea's universities, for instance, have Technology Licensing Offices that facilitate spin-offs – some even have their own venture funds. The Korean Intellectual Property Office (KIPO)'s Intellectual Property Profit Reinvestment Support

Program formerly the Korean Patent Gap Fund Creation Project was launched to narrow the divide between technologies produced in universities and the readiness level expected by industry.[49] This initiative provides substantial early-stage investments in technologies that are still at the research-paper or experimental phase. By financing prototype development, performance testing and certification, and standard patent filings, the program spurs companies to pursue technology transfers more actively. To promote revenue-oriented patent management in academia and public research institutes, KIPO introduced the Institution of Outstanding Patent Quality Management designation in 2020.

Entrepreneurship-in-training

Cultivating an entrepreneurial mindset is essential to grow a local fabless design and IP start-up ecosystem. Entrepreneurship training fosters the ability to turn ideas into impactful products and solutions an essential mindset not only for launching new ventures but also for driving innovation and growth within existing firms. Global experience shows that many semiconductor leaders emerge from strong start-up cultures – new firms that design chips, develop EDA tools, or offer niche IP can propel the industry forward. Viet Nam is positioning the private sector as the engine of innovation: the Politburo s Resolution 68/NQ-TW (May 2025) explicitly elevates private enterprises as "the heart of the national economy" and sets targets to reach two million active firms by 2030.[50] In this context, infusing entrepreneurship into semiconductor training programs will help translate talent into tech start-ups.

Undergraduate and graduate programs should include "entrepreneurship-in-training" modules, such as business plan competitions or incubator practicums focused on chip design and related deep-tech ventures. The Vietnam National Innovation Ecosystem initiative spearheaded by the NIC and leading business schools (e.g., National Economics University, Foreign Trade University) can join forces with the leading tech universities to provide a supportive framework. This addition, either here or under Pillar 1 (Intervention 5), would give promising trainees a pathway to launch semiconductor-related start-ups (e.g., a novel IP core design or an AI-chip prototype) with initial micro-grants and mentoring. The expected payoff is twofold: students gain entrepreneurial skills, and some ventures may mature into new local companies seeding Viet Nam s semiconductor IP ecosystem.

Startup vouchers

Startup vouchers or seed grants should be offered to teams emerging from universities that seek to commercialize semiconductor-related innovations. For instance, if a group of students or a professor has a promising idea (e.g., a new IoT chip, a testing service), they could apply for a US$15,000 $50,000 voucher to cover early-stage expenses such as market studies, prototyping, or patent filing. This initiative could be linked to Viet Nam s broader startup ecosystem support. The goal is to translate research and skills being developed into new ventures, which in turn retain talent domestically and create high-tech jobs. Over time, such efforts could lead to the emergence of homegrown fabless design startups or specialty materials companies from university campuses.

International experience from East Asia underscores the value of such support. Economies such as South Korea, China, Taiwan (China), and Malaysia have implemented targeted startup funding programs to successfully foster university spin-offs and IP-based semiconductor ventures. These schemes typically provide small grants (less than US$50,000) for early-stage needs – from prototyping and patent filing to initial market validation. These are signs of a healthy innovation ecosystem on the university side.

---

49 KAIST. (2020, August 18). KAIST technology value tops in commercialization market. Retrieved from https://news.kaist.ac.kr/newsen/html/news/?mode=V&mng_no=9490

50 Communist Party of Viet Nam. (2025, May 4). Resolution No. 68-NQ/TW of the Politburo on Private-Sector Development. Retrieved from https://baochinhphu.vn/toan-van-nghi-quyet-so-68-nq-tw-ve-phat-trien-kinh-te-tu-nhan-102250505122337909.htm

A voucher focused on talent-rich university teams achieves two goals: (i) it converts the expanding pool of MSc/PhD chip designers into founders rather than footloose employees, and (ii) it keeps public support modular – small enough for quick wins but scalable as the pipeline deepens. A Vietnamese university lab might co-develop a new chip IP that gets licensed to a company; a startup spun off from a university might be acquired by a multinational; or every semiconductor company might regularly source ideas and talent from a partner university, where each department has at least one significant industry project. International evidence suggests that 30–40 percent of voucher recipients reach seed funding within 24 months – a conversion rate well above that of untargeted SME grants. For Viet Nam, even issuing 200 vouchers per year would cost less than 0.1 percent of projected STI spending, yet could seed the country's first wave of homegrown ASIC/IP design firms.

3.3. "VITALS" Program and pilot-line innovation hubs

Viet Nam may consider a Vietnam Innovation & Talent Alliance for Semiconductors (VITALS) initiative in the medium-to-long term to systemically break down the silos and accelerate knowledge spillovers between academia and industry and between FDI firms and local firms. This initiative can offer co-funding grants for projects that pair large multinational companies with Vietnamese SMEs, suppliers, or universities. The goal is to localize knowledge, develop supply chains, and foster technology transfer from anchor investors to Vietnamese firms and workers.

VITALS may cover various partnership modalities - from supplier development and co-innovation projects to workforce upskilling – and would ensure that innovations and process know-how from MNCs spill over to the local industry. Another use case could be funding joint company–university "demonstration" projects (e.g., a company testing a new chip design in a university lab). It can also provide incentives for an FDI semiconductor firm to mentor and upgrade a group of domestic suppliers (materials, components, services) with government grants matching a portion of the firm's investment in the partnership. By structuring the initiative's funding windows, the government can systematically "keep spillovers local," ensuring that advances introduced by global players result in Vietnamese engineers and firms gaining new capabilities.

Concretely, the program could be coordinated by the Ministry of Industry and Trade (MOIT) or the NIC, with cost-sharing grants (e.g., covering approximately 50 percent of project costs up to a cap) and clear deliverables (such as the number of local staff trained, new processes adopted, or IP shared). Over time, this will build a network of Vietnamese suppliers and start-ups integrated into global semiconductor value chains.

This VITALS can also include as its components the establishment of "open" innovation hubs where academia and industry co-create. As discussed under the Pillar 2 on infrastructure, a key recommendation is to establish shared pilot production lines in strategic areas like advanced packaging. Such a facility – potentially set up via a public–private partnership with industry partners – would house state-of-the-art bonding, lithography, and metrology equipment for 2.5D/3D packaging, accessible to researchers and firms for prototyping new solutions. The benefit is twofold: workforce upskilling on real industrial equipment and innovation testing without disrupting high-volume production lines. Global models – such as Belgium's imec and Japan's National Institute of Advanced Industrial Science and Technology/LSTC – show that neutral R&D hubs operated as consortia can catalyze an entire ecosystem. Similarly, an IC design and prototyping "commons" (design hub) with cloud-accessible EDA tools and multi-project wafer services, as discussed under Pillar 1, would lower barriers for start-ups and universities to fabricate test chips.

As discussed in Section 2.4, these centers should co-locate academic and industry talent and be co-funded by public and private partners over the medium to long term. Singapore's new National Semiconductor Translation & Innovation Centre (NSTIC) is a S$180 million (US$135 million) facility that provides companies and researchers with shared cleanrooms, industry-grade tools, and onsite experts to accelerate

translational R&D. Companies can use NSTIC for small-volume manufacturing and then smoothly transfer processes to commercial fabs. Viet Nam's pilot-line hubs could play a similar role – serving as a sandbox where university teams, local start-ups, and foreign firms collaborate on experimental new designs or processes (e.g., a silicon photonics lab or a MEMS foundry, at smaller scale). To encourage utilization, the government might subsidize access for universities and SMEs and require any firm receiving incentives (tax breaks, R&D grants) to participate in these shared facilities or associated training programs. Over time, these innovation hubs will help root more R&D activity in Viet Nam – a critical step, since companies ultimately go where the talent and capabilities are.

This suite of investments would create a bridge from research to commercialization, and from MNCs to local capacity, that is currently missing. Local SMEs and academia would gain hands-on experience with frontier technologies, increasing the likelihood that the next big idea in semiconductors could be developed and commercialized domestically. These initiatives complement the matching grants and start-up supports described above – collectively moving Viet Nam closer to a full-fledged innovation ecosystem for semiconductors. They also incentivize overseas Vietnamese experts and foreign firms to base more R&D in Viet Nam, knowing there is an enabling environment of talent, facilities, and collaboration programs. In sum, catalyzing university–industry–government innovation will ensure that Viet Nam not only trains more engineers (Pillar 1) and builds labs (Pillar 2), but also harnesses those inputs to produce intellectual property, high-tech start-ups, and value-added jobs at home.

4. GOVERNING AND FINANCING MECHANISMS FOR IMPACT AT SCALE

To tie everything together, Viet Nam needs effective governance and financing mechanisms. This pillar focuses on how to manage the multi-faceted program and secure sustainable funding, with clear accountability for outcomes. In essence, it addresses who will drive this agenda, how it will be coordinated, and how it will be paid for.

4.1. Establish a steering and governing body for semiconductor talent development

Given the complexity and strategic importance, there should be a dedicated Semiconductor Talent Governing Body as the central steering and troubleshooting authority to steer this agenda. This body could function as a sub-committee under the National Steering Committee on Science, Technology, Innovation, and Digital Transformation, and should ideally be chaired at the highest possible level of state leadership. Membership should include representatives from key ministries (MOET, MOST, MOF), industry leaders, and representatives from Viet Nam's leading universities.

High-level state or government leadership would signal the priority attached to this agenda. The governing body would function as an apex decision-making entity to break down silos between education, STI, and industrial policies. It could include an advisory group of industry leaders and university rectors, mirroring South Korea's Presidential STI Advisory Council, to institutionalize public–private dialogue on skills needs. By providing strategic direction for semiconductor talent development, and by overseeing a unified action plan and results framework, the Council would ensure coordinated implementation across stakeholders and rapid resolution of issues such as funding delays or curriculum approvals. To ensure that strategic direction is properly and promptly acted upon, a supporting secretariat or delivery unit with adequate resources and staffing should be established.

In Singapore, the Singapore Economic Development Board (EDB) - the government's industry development agency under the Ministry of Trade & Industry - serves as the de facto convener linking talent-policy instruments (e.g., scholarships, conversion programs, manpower regulations) with innovation levers (e.g., public R&D funding, pilot-line infrastructure, corporate co-investment schemes) for the semiconductor sector.[51] EDB leads the multi-agency Electronics Industry Transformation Map refresh, aligning jobs-and-skills initiatives with R&D and investment roadmaps. Practical programs – such as the IPP, IC Design Summer Camp, and Career Conversion Schemes – are delivered through close partnerships between EDB, institutes of higher learning, SSIA, and industry players to feed the semiconductor talent pipeline that underpins ongoing R&D expansion. In effect, the agency serves as a single point of accountability for companies and universities that require both skilled personnel and an innovation ecosystem. From heterogeneous-integration centers of excellence to the national NSTIC pilot fab, EDB ensures that talent supply, research infrastructure, and investment incentives move in lockstep across Singapore's semiconductor value chain.[52]

4.2. Integrate and leverage financing streams: a one-stop platform

Viet Nam has multiple funding sources to support an integrated agenda for semiconductor talent development and R&D, with different public versus private financing shares. The ISF provides subsidies

[51] Singapore EDB. (2023, February). EDB Year 2022 in Review. Retrieved from https://www.edb.gov.sg/en/about-edb/media-releases-publications/edb-year-2022-in-review.html

[52] Singapore Economic Development Board. (2024, March 12). What makes Singapore a prime location for semiconductor companies driving innovation. Retrieved from https://www.edb.gov.sg/en/business-insights/insights/what-makes-singapore-a-prime-location-for-semiconductor-companies-driving-innovation.html

and reimbursement for firm-based upskilling, echoing models implemented elsewhere. The ISF – if capitalized with several hundred million US$ initially – and the anticipated National Program on Strategic Technology & Industry Development (NPSTID) and Strategic Industry Development Investment Fund (SIDIF) would provide significant funding for tech talent development. These can be directed not only toward infrastructure but also toward talent development matching schemes. A portion of the ISF, NPSTID, and SIDIF could be specifically dedicated to semiconductor talent non-infrastructure activities.

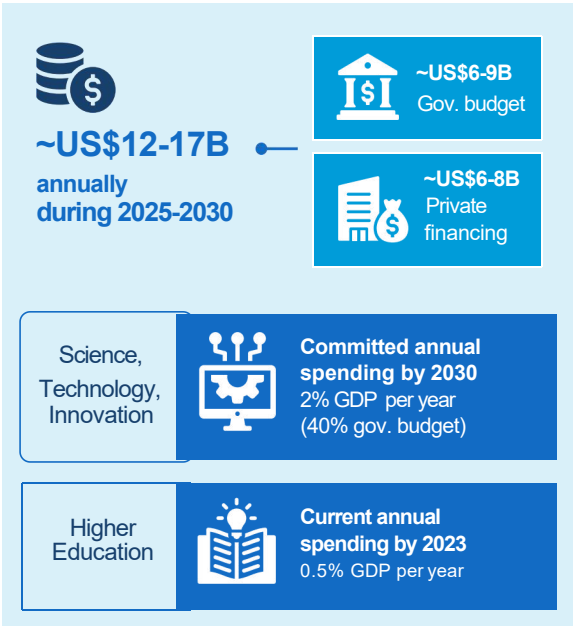
These resources should be coordinated under a common umbrella rather than remainsiloed to improve accessibility, efficiency, and utilization. For example, a one-stop-shop funding platform could combine various streams and use them to co-finance strategic projects. While formal consolidation and full integration are difficult, a joint steering mechanism between MOET, MOST, and the managing agencies of the related funds could align their programs. On such a platform, the funding line agencies could jointly issue annual calls for proposals, where consortia of universities and firms apply for funding for integrated initiatives. The education budget could fund the university training costs, the Investment Fund could support the industry portion, the Infrastructure Fund could support high-impact, large-scale infrastructure, and MOST could top up for R&D capacity building – all evaluated in a single process. This approach ensures that public funds crowd in private investment on the same projects, rather than fund things separately. In essence, pooling funds around common objectives on a unified platform would be critical for maximizing impact and ensuring coherence across Viet Nam' s semiconductor talent and innovation financing landscape.

5. COST, IMPLEMENTATION, RISKSAND OPPORTUNITIES

Having outlined the what of the strategy, we turn to the how much, how and when, and what if aspects – essentially the financing envelope and phasing (the cost and timeline), how to structure implementation, and an assessment of key risks with mitigation measures.

5.1. Envelope & phasing 2025-2030

Figure 30. Financing commitment for the STI and university agenda



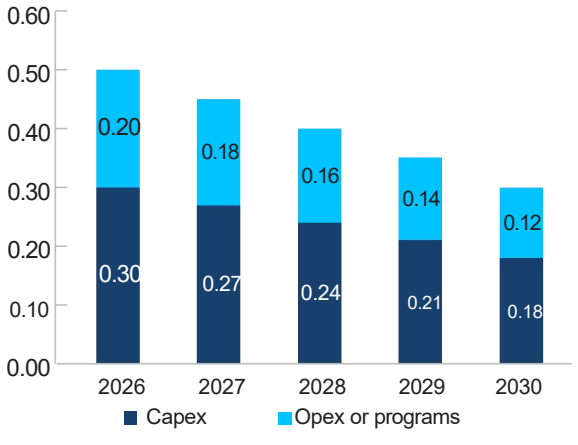
Investment envelope

We estimate that implementing this talent agenda will require, at the minimum, US$2 billion over 2026–2030. This figure includes both capital expenditures (capex) for infrastructure and ongoing program costs (operational expenditures, opex). It encompasses government spending, private sector contributions, and potential donor financing. For perspective, US$2 billion over 5 years is substantially lower than the commitment by regional peers and roughly 0.1–0.2 percent of Viet Nam' s GDP per year – a manageable sum considering the strategic importance and expected returns (high-skill jobs, FDI attraction, etc.) (Figure 30).

Cost breakdown: capex versus opex

About 40 percent, approximately US$ 0.8 billion, would cover opex/ non-infrastructure programs – scholarships and stipends, training program delivery, research grants, etc – dominated by government funding. The remaining roughly 60 percent of the envelope would likely go to capex – building and equipping labs, centers of excellence, digital infrastructure (EDA cloud, etc.) (Figure 31). In practice, capex will be front-loaded in the early years (build the facilities, establish programs) and opex will be recurrent throughout (funding scholarships annually, maintaining labs, etc.).

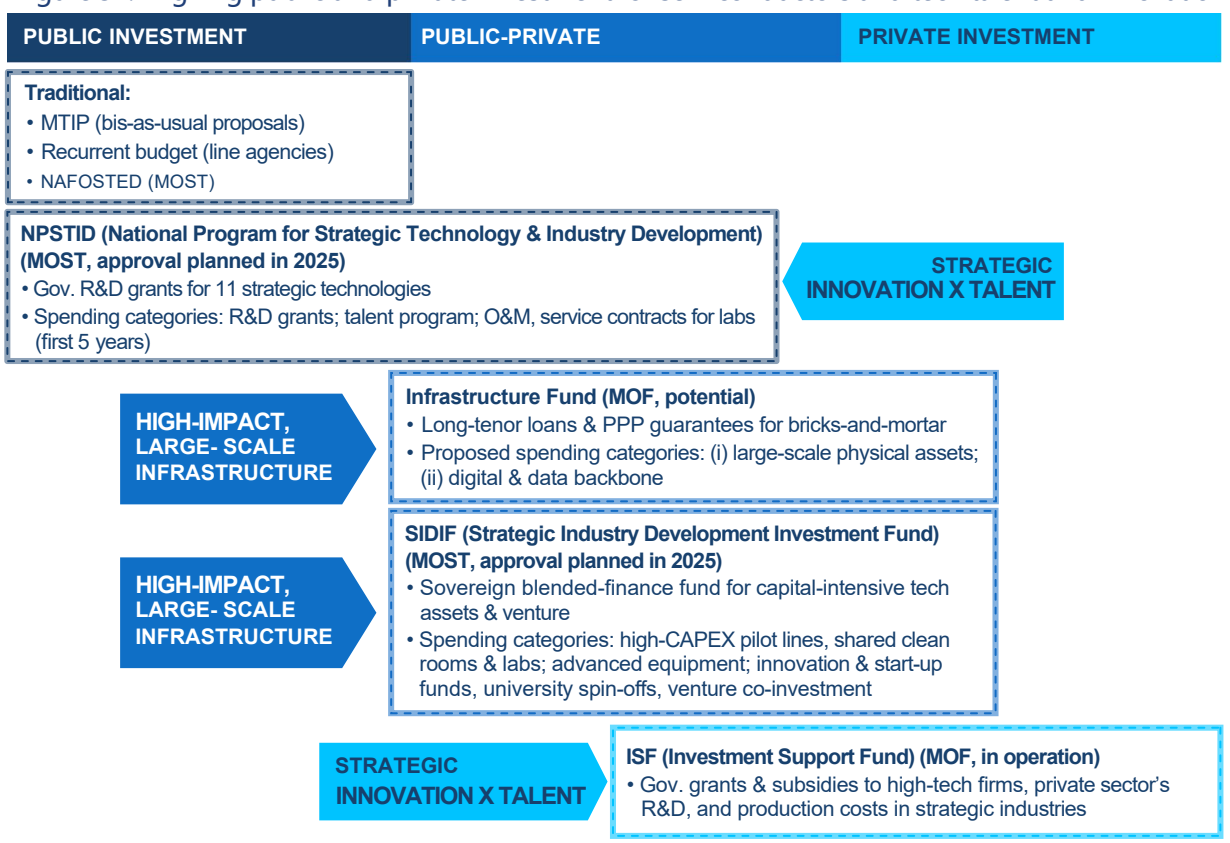
Figure 31. Proposed breakdown of annual expenditure, 2026-2030 (US$ billion)



Public–private split

The program is designed with phased co-financing. It is proposed that the public sector (government and donor) would fund about 50 percent of the total (approximately US$2 billion), and the private sector about 50 percent in the first 3-5 years and gradually increase to 60 percent. Early on, the government may shoulder a larger share (perhaps 60 percent in 2026–27) as infrastructure and non-infrastructure program setups are largely publicly funded. But as we roll out matching schemes and as industry starts using facilities, the private contribution should rise (potentially surpassing 60 percent in later years). By 2030, the goal is that for every dollar the government spends on semiconductor talent, the private sector is also spending a dollar – whether through cost-share on labs, training their staff, or sponsoring university programs.

Figure 32. Aligning public and private investment for semiconductors and tech talent and innovation



Source: World Bank staff compilation based on Politburo Resolution 57-NQ/TW, Decree 182/2024/ND-CP, Prime Minister Decision 1131/QD-TTg, Government Office 171/TB-VPCP.

Note: MTIP for Mid-Term Investment Plan. NAFOSTED for National Foundation for Science and Technology Development. O&Mfor operations and maintenance. HPC for high performance computing. CAPEX for capital expenditure.

In-kind contributions, such as industry donation of used equipment or the provision of experts (worth monetary value), should be counted toward the private share. The state budget portion will come from MOET (education) funds, MOST (science & tech) funds, and central programs and related funds. We assume the government incrementally increases annual budget allocations to these efforts, leveraging the country's fiscal space (public debt is relatively low, and investing additional 0.2 percent of GDP in HE, from the current low base of 0.35-0.45 percent of GDP, is justified by growth dividend).

Overall, the US$2 billion package over five years is ambitious but feasible. Viet Nam's fast growth and fiscal space (public debt on a downward path, potential to increase public investment by approximately 2 percent of GDP according to analyse) provide room. Moreover, by designing many elements as cost-sharing with private sector, the burden on state coffers is moderated and the effectiveness of spending is heightened.

5.2. Risks and mitigation measures

No ambitious program is without risks, but all considered, most risks as moderate and manageable with the proposed mitigations. We identify several key risks along with corresponding mitigations, as well as some opportunities that could be capitalized on. The highest risk is arguably brain drain; however, given the strong demand for skilled engineers in Viet Nam (and cultural ties), many trained individuals will have the incentive to stay if decent opportunities exist. Frequent monitoring by the Talent Council will ensure that if any risk indicator starts turning red (e.g., more than 20 percent of scholars not returning), immediate action can be taken (maybe bonding requirements made stricter or salaries adjusted). By anticipating these issues now, Viet Nam can implement this ambitious program with confidence and agility.

Risk 1: Brain drain

A top risk is that after investing in advanced training (Master's, PhDs), individuals may choose to leave Viet Nam for higher salaries or opportunities abroad. This would undercut the local talent pool.

Mitigations: Implement bonding agreements for scholarship recipients those funded for study abroad or expensive programs commit to work in Viet Nam for a minimum period (e.g., 3-5 years) or pay back a portfolio. Additionally, improve local incentives: create attractive R&D positions and career pathways domestically (as earlier noted, establish research institutes, labs, or encourage multinationals to open R&D offices in Viet Nam that employ these returning scholars). Diplomatic channels can also be established to create "brain circulation" instead of one-way brain drain e.g., engaging diaspora to remain involved in Viet Nam s projects even if physically abroad. Finally, closely monitor retention rates; if certain programs see high exit rates, adjust the selection or bonding accordingly.

Risk 2: Fiscal stress or funding shortfall

If economic conditions change or government priorities shift, there is a risk that the planned public funding (especially the large US$2 billion envelope) might not fully materialize. There could be budget cuts or reallocation away from education/STI if fiscal pressures rise.

Mitigations: Secure strong political commitment (through Resolution and multi-year budget earmarks) upfront to protect this program as a priority. Moreover, phase the project into scalable segments if less funding is available, core elements (like scholarships and critical labs) get priority, and lower-priority or more experimental initiatives can be deferred or downsized. Embedding private sector co-financing and exploring alternative funding (like university endowment contributions, philanthropic funds) can also reduce reliance on the state budget. Another mitigation is demonstrating early results to maintain political support if by 2027 the program shows clear successes (jobs created, investors attracted), it is less likely to face cuts.

Risk 3: Demand shocks or market volatility

The semiconductor industry is cyclical and technology evolves rapidly. There's a risk that the skills being developed could face lower demand if the market shifts – for example, a global downturn in chip demand might slow hiring, or a new technology might change the skillset required (e.g., a move to AI-designed chips or quantum computing in the far future).

Mitigations: Design the curriculum and training with flexibility and breadth and a principle of "no-regret". Focus on fundamental skills (solid electronics engineering, problem-solving, programming) that are transferable even if specific technologies change. Also continuously update programs based on industry feedback each year (the Industry Advisory Boards will help detect shifts in skill needs and can suggest curriculum tweaks in near real-time). If a cyclical downturn occurs (e.g., graduates do not immediately find jobs due to a temporary slump), use that time productively: encourage graduates to pursue further specialization (PhD, research) during the lull, or temporarily absorb them into public research projects until the market picks up. Essentially, avoid over-specialization in a narrow technology and maintain an agile training system that can pivot as needed.

Risk 4: Private sector participation risk

There is a risk that companies might not show up to the extent expected – perhaps due to lack of awareness, trust, or their own constraints – jeopardizing the feasibility of the plan which banks on significant private sector co-investment and engagement.

Mitigations: Intensive early engagement and communication with industry is key. Through the Council and industry associations (like electronics associations), socialize the program and its incentives. Simplify processes for firms to participate (e.g., easy application for matching grants, minimal red tape for setting up joint labs). Demonstrate quick wins – e.g., highlight a success story of one company that got a 50 percent grant to upgrade a training center, to motivate others. If necessary, adjust incentive levels – for instance, if initial uptake of matching grants is low, consider increasing the government match temporarily or expanding eligibility. Also involve some flagship investors (Intel, Samsung, etc.) early so that SME suppliers follow their lead.

REFERENCES

Agency for Science, Technology and Research (A*STAR). 2024. National Semiconductor Translation and Innovation Centre (NSTIC): Factsheet. Singapore.

Afreen Siddiqi. 2022. “A Brief Introduction to Systems Thinking.” Harvard Kennedy School.

Alok Medikepura Anil. 2025. “Technology Convergence Is Leading the Way for the Fifth Industrial Revolution.” World Economic Forum, 13 Jan 2025.

Amkor Technology. 2023. Amkor Opens US $1.6 billion Advanced SiP ‘Smart Factory’ in Bắc Ninh, Việt Nam. Press release, 7 Nov 2023.

Bentil, E. et al. 2025. Assessment of infrastructure gaps and priority investments for Viet Nam National University Ho Chi Minh City.

Boston Consulting Group (BCG). 2022. The Growing Challenge of Semiconductor Design Leadership. Boston.

Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA). 2020. Government Incentives and U.S. Competitiveness in Semiconductor Manufacturing. Washington DC: SIA.

Boston Consulting Group (BCG) & Semiconductor Industry Association (SIA). 2021. Strengthening the Global Semiconductor Value Chain in an Uncertain Era. Washington DC: SIA.

China Center for Information Industry Development (CCID) & China Semiconductor Industry Association (CSIA). 2023. White Paper on Talent: China’s Integrated-Circuit Industry (2022-2023). Beijing: CCID Press.

Dang, V. Q. et al. 2025. Promoting university R&D and technology transfer for productivity growth in Viet Nam.

Dao, T. H. et al. 2025. Skilling up for Viet Nam’s semiconductor industry: Assessing talent gaps and higher education capacity.

Deloitte. 2022. The Global Semiconductor Talent Shortage: Preparing for the Next Wave. New York.

Deloitte. 2023. 2024 Global Semiconductor Industry Outlook. New York: Deloitte Insights.

Donella H. Meadows. 2008. Thinking in Systems: A Primer. White River Junction: Chelsea Green.

Draghi, M. 2024. The Future of European Competitiveness: In-depth Analysis and Recommendations (Part B). Report to the European Commission, Sept 2024.

FUV (Fulbright University Việt Nam). 2024. Việt Nam Semiconductor Workforce Development – Final Report. 15 Nov 2024.

General Statistics Office of Việt Nam (GSO). 2025. Statistical Yearbook of Việt Nam 2024. Hà Nội.

General Statistics Office of Việt Nam (GSO). Annual. Labour-Force Survey Micro-data 2013-2023. Hà Nội.

Rosenbach, E. et al. 2025. Critical and Emerging Technologies Index. Cambridge MA.

International Finance Corporation (IFC). 2020. Việt Nam Electronics & Electrical-Equipment Value-Chain Study (internal working paper). Washington DC.

International Monetary Fund (IMF). 2023. World Economic Outlook – April 2023: A Rocky Recovery. Washington DC.

International Monetary Fund (IMF). 2025. Industrial Policies: Handle with Care. Staff Discussion Note SDN/25/01. Washington DC.

Jeremy Jurgens & Kary Bheemaiah. 2025. "Rhythms of Innovation: How Technology Synergies Are Redefining the Future." World Economic Forum, 21 Jan 2025.

Korea Semiconductor Industry Association (KSIA). 2022. "Response of KSIA to U.S. CHIPS Incentives Program Request-for-Information." Seoul.

Korea Semiconductor Industry Association (KSIA). 2023. "SEDEX Report – 25th Semiconductor Exhibition Overview." Seoul.

McKinsey & Company. 2024. Will the World Have Enough Chip Engineers after 2030? Semiconductor Practice Insight, Jan 2024.

Ministry of Science & Technology (MOST) Việt Nam. 2024. Science, Technology and Innovation Indicators of Việt Nam 2023. Hà Nội.

Ministry of Trade & Industry Singapore. 2024. Enhanced PACT Scheme: Factsheet.

National Science Foundation (NSF). 2024. Doctorate Recipients from U.S. Universities: 2023 Data Tables. Alexandria VA.

National Science Foundation (NSF). 2025. Engineering Research Centers (ERC) Program Overview. Arlington, VA: U.S. National Science Foundation.

Nguyen, M., Tran, H. L. T., & Bergman, J. B. 2025. Viet Nam semiconductor industry rapid assessment.

NSTIC. 2024. Factsheet for COS 2024. National Semiconductor Translation and Innovation Centre, Singapore.

OECD. 2015. Frascati Manual 2015: Guidelines for Collecting and Reporting R&D Data. Paris.

OECD. 2024a. Chips, Nodes and Wafers: A Taxonomy for Semiconductor Data Collection. Paris.

OECD. 2024b. Promoting the Growth of the Semiconductor Ecosystem in the Philippines. Paris. doi: 10.1787/01497fea-en.

Park, Suzy E. 2019. Technological Convergence: Regulatory, Digital Privacy and Data Security Issues. Congressional Research Service, 30 May 2019.

RAND Corporation. 2024. Structures, Functions, and Processes of Centers of Excellence. Santa Monica, CA: RAND Corporation.

Semiconductor Industry Association (SIA). 2023. State of the U.S. Semiconductor Industry 2023. Washington DC.

SIA. 2024. SIA 2024 Factbook. Washington DC.

SIA & Boston Consulting Group (BCG). 2024. Emerging Resilience in the Semiconductor Supply-Chain. Washington DC: SIA.

SIA & BCG. 2021. Strengthening the Global Semiconductor Supply Chain in an Uncertain Era. Washington DC: SIA.

SIA & BCG. 2020. Government Incentives and U.S. Competitiveness in Semiconductor Manufacturing. Washington DC: SIA.

SIA & Oxford Economics. 2023. Chipping Away at the Gap: America's Semiconductor Workforce Needs. Washington DC: SIA.

USAID. 2024. Semiconductor Education and Skills Analysis Brief. USAID/Vietnam Higher Education Development Support Activity. Unpublished.

World Bank. 2020a. Việt Nam: Science, Technology and Innovation Report. Washington DC.

World Bank. 2020b. Improving the Performance of Higher Education in Việt Nam. Washington DC.

World Bank. 2021. Việt Nam: Adapting to An Aging Society. Washington DC.

World Bank. 2023a. Policy note on "Higher Education Financing in Vietnam: Strategic priorities and policy options". Washington DC.

World Bank. 2023b. Promoting Innovative Entrepreneurship in Viet Nam. Washington DC.

World Bank. 2024a. Việt Nam 2045 – Trading Up in a Changing World: Pathways to a High-Income Future. Washington DC.

World Bank. 2024b. East Asia & Pacific Economic Update – October 2024: Jobs and Technology. Washington DC.

World Economic Forum. 2024. Technology Convergence 2024: Synergies between AI, Semiconductors and Frontier Tech. Geneva.

World Intellectual Property Organization (WIPO). 2024. Global Rankings of Science & Technology Clusters: Annex to the Global Innovation Index 2024. Geneva.

Singapore Economic Development Board (EDB). 2024. "What Makes Singapore a Prime Location for Semiconductor Companies Driving Innovation." EDB Insights

ANNEX

ANNEX 1. GLOSSARY OF TERMS

Term/ Acronym	Concise meaning & Viet Nam relevance
Advanced Packaging (AP)	A new generation of chip packing technologies – e.g., 2.5D/3D integration, fan-out wafer-level, chiplet stacking – that combine multiple chips and functions into one high-performance unit. AP enables fast, low-power chips that can process large volumes of data for key applications like automotive computing, generative artificial intelligence (AI), 5G, electric vehicles (EVs), and Internet of Things (IoT). AP doubles today's US$48 billion market by 2030 and is already being piloted by Intel and Amkor plants in Viet Nam, offering a springboard into higher value manufacturing.
Application-Specific Integrated Circuit (ASIC)	A custom chip optimised for one task (AI inference, 5G base-band, power management, etc.). Global demand is surging; Viet Nam's design houses can capture niches by moving from generic back-end services to full ASIC intellectual property (IP) creation.
Assembly, Test & Packaging (ATP)	The traditional back-end segment that attaches the finished dies to packages, wires them, and tests their functionality. Viet Nam hosts Intel's largest ATP site and multiple foreign outsourced semiconductor assembly and test (OSAT) plants, supplying thousands of technician and engineer jobs.
BiCMOS / FinFET / CMOS nodes	A node refers to a chip manufacturing generation – how small the transistors are – measured in nanometers (e.g., 3nm, 2nm). Smaller nodes enable faster, more power-efficient chips. CMOS is the basic transistor type used in most chips, but as it gets smaller, it starts to leak power. FinFET is a newer 3D design that reduces power loss and improves performance, especially important for advanced chips like AI and mobile devices. BiCMOS combines digital CMOS with special analog parts that handle real-world signals like sound, radio waves, or power – used in 5G, radio frequency (RF), and power management chips. Understanding how these technologies affect chip behavior is essential for designing reliable, high-performance circuits. Mastery of these nodes is required for front-end integrated circuit (IC) design and is a current skills gap in Vietnamese curricula.
Chiplet	A small functional die designed to be combined with others in one package via AP; enables faster time-to-market and heterogeneous integration. Driving demand for AP capacity in Viet Nam.
Cleanroom	Controlled-environment facility (class 10–1000) required for wafer processing and some AP steps; shared pilot lines are recommended for universities/industry to prototype without building full fabs.
Design Technology Co-Optimisation (DTCO)	Concurrent optimisation of IC layout and package/board design to meet power-performance-area targets. Close IC-design/AP interaction in Viet Nam can create differentiated solutions as local capability matures.
Discrete, Analog & Other (DAO) devices	Diodes, sensors, power-management and RF parts that translate, condition or switch signals and power; together with logic & memory they complete electronic systems. DAO shares are growing in EVs and IoT, opening design & test niches for Vietnamese firms (definition adapted from report image).

Term/ Acronym	Concise meaning & Viet Nam relevance
Electronic Design Automation (EDA)	Software tool chains (Cadence, Synopsys, Siemens, etc.) that automate the chip and printed circuit board (PCB) design process – from register-transfer level (RTL), which defines early logic, to the final manufacturing layout (GDSII). Tool proficiency is a minimum hiring criterion and the subject of multiple memorandums of understanding (MoUs) between Vietnamese universities and vendors.
Front-end versus Back-end Design	Front-end covers system architecture (overall function), micro-architecture (functional blocks and data paths) and RTL/analog circuit invention (logic behavior and signal handling) – largely human-driven and research-intensive; back-end consists of physical implementation and verification tasks that are increasingly automated by AI. Viet Nam is strong in back-end but must up-skill for front-end roles to create IP.
Foundry	A contract wafer-fabrication plant (e.g., TSMC, Samsung Foundry) that manufactures designs from fabless customers. Viet Nam currently lacks foundry capacity; policy focuses on design/AP strengths that dovetail with foreign foundry ecosystems.
Integrated Circuit (IC)	A set of electronic components patterned on a semiconductor wafer. When packaged it becomes a chip that powers electronic products. The IC value chain stages – design, wafer-fab, ATP, AP – determine where Viet Nam can add value.
Logic Semiconductor	Processor or controller chips that execute instructions – the "brains" of computing – from micro-controllers to AI accelerators. Highest value segment for design talent; long-term ambition for Vietnamese fabless start-ups.
Memory	Chips that store data/instructions, including DRAM (short-term working memory), NAND (long-term storage), MRAM (fast, durable next-gen memory). Packaging & test requirements for high-bandwidth memory (HBM) drive AP investments such as Amkor's SiP line in Bac Ninh.
Multi-Project Wafer (MPW) / Design commons	A shared shuttle service where multiple designs are pooled onto one wafer run, cutting prototype costs for universities and SMEs. Recommended as part of a national IC-design & prototyping "commons".
OSAT (Outsourced Semiconductor Assembly & Test)	Specialist companies (e.g., Amkor, JCET, Hana Micron) that package and test chips for fabless/foundry clients. Viet Nam's existing OSAT base is a cornerstone for expanding into AP.
Pilot Line / Tech Center	A shared research and development (R&D) production line (often public-private) that lets researchers and firms trial new processes on industry-grade tools – e.g., an Advanced Packaging Tech Center proposed for Viet Nam by 2026.
System-in-Package (SiP)	An AP approach that integrates multiple ICs and passive components inside one module for size/performance gains – focus of Amkor's new "smart factory" in Viet Nam.
System-on-Chip (SoC)	A single chip that integrates multiple system functions – such as processing, memory, and connectivity – onto one piece of silicon. Their complexity requires advanced front-end design skills, which Viet Nam is beginning to build through partnerships and education programs aimed at higher-value semiconductor design.

ANNEX 2. UNIVERSITIES IN EAST ASIA WIPO GLOBAL TOP 100 SCIENCE AND TECH CLUSTERS

East Asia's science-and-technology (S&T) clusters almost always coalesce around a flagship research university (or compact group of universities) that acts as the anchor for talent, basic research, and spin-off activity.

- China's two biggest hubs — Shenzhen-Hong Kong-Guangzhou and Beijing — are characterized by a concentration of universities, including Shenzhen University, the Hong Kong universities, and SUSTech in the Pearl River Delta, together with Tsinghua and Peking University in the capital. Wuhan and Hangzhou follow the same model: Huazhong University of Science & Technology and Zhejiang University each sit at the centre of local optics-electronics and AI semiconductor corridors.
- South Korea's four WIPO-listed clusters are likewise university-centred: Seoul-Incheon around Seoul National University and the "Techno Valley" of Yonsei and Korea University.
- Taiwan (China)'s single global top-100 cluster, Hsinchu, is literally built around National Tsing Hua and (Yang Ming) Chiao Tung Universities, whose joint graduate programs feed directly into TSMC and the Industrial Technology Research Institute (ITRI).
- Singapore's cluster is anchored by the National University of Singapore and Nanyang Technological University, whose shared research parks (CREATE, Fusionopolis) host imec, Applied Materials and chip-design startups.

Across these hubs, universities perform three roles: (i) they generate frontier knowledge through state-funded and industry-sponsored labs; (ii) they supply a continuous pipeline of specialised human capital — especially Master's and PhD engineers that staff corporate R&D; and (iii) they serve as neutral conveners, running technology parks and incubators that enable startups and multinationals to co-locate and share prototyping facilities. This tight university-industry coupling is a critical determinant for East Asia's 36 of the world's top 100 S&T clusters — 26 in China, 4 in South Korea, 3 in Japan, and one each in Taiwan (China), Singapore, and Malaysia.

Table A1. Major East Asian S&T clusters and their academic & R&D anchors

The table focuses on China's top five clusters plus all WIPO-listed clusters in South Korea, Japan, Taiwan (China), Singapore, and Malaysia.

Country / Cluster (WIPO 2024 rank)	Anchor research universities	Key university-industry science parks / joint centres	National labs & flagship public R&D institutes
China (Top 5/26 only)			
1. Shenzhen Hong Kong Guangzhou	SUSTech; Shenzhen University (U.); HKU & HKUST; South China U. of Technology.	Shenzhen High-Tech Park; Qianhai Shenzhen-HK Sci Tech Zone; Guangzhou-HK Science & Innovation Corridor	National Super-computing Center (Shenzhen); CAS Shenzhen Institutes; Huawei SUSTech Joint IC Lab
2. Beijing	Tsinghua U.; Peking U.; Beihang U.	Zhongguancun Science Park; Tsinghua x-lab; PKU Founder Park	National Lab for Information S&T; Institute of Micro-electronics CAS; Beijing Academy of AI
3. Shanghai Suzhou	Fudan U.; Shanghai Jiao Tong U.; Soochow U.	Zhangjiang Hi-Tech Park; Suzhou Industrial Park-Nanopolis	Shanghai Synchrotron Radiation Facility; National IC Innovation Center; CAS Shanghai Micro-systems Inst.

Table A1. Major East Asian S&T clusters and their academic & R&D anchors (continued)

Country / Cluster (WIPO 2024 rank)	Anchor research universities	Key university-industry science parks / joint centres	National labs & flagship public R&D institutes
4. Nanjing	Nanjing U.; Southeast U.; Nanjing U. of Science & Technology	Nanjing Jiangbei New Area Sci–Tech Park; Nanjing High-Tech Industrial Zone	Purple Mountain Observatory; CAS Nanjing Institute of Geo-Engineering; State Key Lab of Bioelectronics
5. Wuhan	Huazhong U. of Science & Technology; Wuhan U.	Wuhan "Optics Valley of China"; HUST-Lenovo Innovation Base	Wuhan National Lab for Optoelectronics (WNLO); National Engineering Research Center for Fiber Optics
South Korea			
Seoul–Incheon	Seoul National U.; Yonsei U.; Korea U.	Gwanggyo & Pangyo Tech Valleys; SNU-Samsung Advanced Institute	Korea Institute of S&T (KIST); Seoul National Super-computing Center
Daejeon (Daedeok Innopolis)	KAIST; Chungnam National U.	Daedeok Innopolis (1,000+ labs & start-ups)	Electronics & Telecommunications Research Inst. (ETRI); KISTI, KRISS
Busan	Pusan National U.; Korea Maritime & Ocean U.	Busan Techno Park	Korea Inst. of Ocean Science & Tech (KIOST)
Ulsan–Pohang	UNIST; POSTECH	Ulsan Techno Park; POSTECH Startup Valley	Pohang Accelerator Laboratory (PAL); IBS Center for Multidimensional Carbon Materials
Japan			
Tokyo–Yokohama	U. of Tokyo; Keio; Waseda U.	Tokyo 'Edge-AI' Startup Hub; Kawasaki Innovation Gateway	RIKEN Center for Advanced Photonics; AIST Tsukuba HQ
Osaka–Kyoto	Osaka U.; Kyoto U.	Kansai Science City (Keihanna)	RIKEN Center for Computational Science (Kobe); AIST Kansai
Nagoya	Nagoya U.; Toyota Tech. Inst.	Aichi S&T Park; Chubu Cent. for Innovation	National Institute for Materials Science - Nagoya branch
Taiwan, China			
Hsinchu Science Park	National Tsing Hua U.; National Yang Ming Chiao Tung U.	Hsinchu Science Park; NTHU-NYCU Joint Micro-Nano Ctr.	Industrial Tech. Research Inst. (ITRI); Taiwan Semi. Research Inst. (TSRI)
Singapore			
Singapore	National U. of Singapore; Nanyang Technological U.	CREATE Campus; Fusionopolis; NUS-imec Nano-electronics Centre	A*STAR Inst. of Micro-electronics; Singapore-MIT Alliance for Research & Tech. (SMART)
Malaysia			
Kuala Lumpur	University of Malaya; Universiti Putra Malaysia; Universiti Kebangsaan Malaysia	Technology Park Malaysia; Cyberjaya Innovation Hub	SIRIM Berhad; Malaysian Institute of Microelectronic Systems (MIMOS); Academy of Sciences Malaysia

Source: WIPO Global Rankings of S&T Clusters 2024. Universities, parks and labs compiled from official cluster and institution websites and national science-agency reports.

ANNEX 3. ESTIMATION OF VIET NAMgS EXISTING SEMICONDUCTOR WORKFORCE

The Table A2 below shows the World Bank s estimation of Viet Nam s existing semiconductor workforce in both ATP and IC design firms.

The labour force currently counts about 17,000 people in mid-2025, split between approximately 7,500-8,000 staff at more than 60 IC design houses (Renesas, Synopsys, FPT Semi, Viettel, etc.), assuming the 3:1 ratio for engineer-to-support staff (FUV 2024); and about 9,000 in back-end ATP plants led by Intel Products Vietnam, Amkor Technology s new Bac Ninh OSAT line and Hana Micron Vina in Bac Giang. All head-count figures include engineers, technicians, production operators, managers and support functions.

Looking forward, two forces drive the estimated workforce jump to roughly 85,000 jobs by 2030: (1) the government s explicit goal of training 50,000 design engineers, which, if the current 3 : 1 engineer-to-support staffing ratio is applied and all of them stay in Viet Nam, lifts the design workforce to about 65,000; and (2) committed OSAT expansions Amkor s complex alone is slated to grow to 6,000-7,000 workers, Hana Micron to 4,000, and new entrants such as Samsung Electro-Mechanics and CT Semiconductor will add several thousand more taking the ATP segment toward 20,000. Together, these top-down (policy) and bottom-up (plant-specific) drivers imply that Viet Nam' s semiconductor workforce will quintuple in five years.

TabIeA2. Viet Namgs existing semiconductor workforce and expansion target

Segment / facility	Province / city	Approximate current head-count* (mid-2025)	Expansion target** (announced estimation)	Notes
IC design houses (appx. 60 firms) e.g., Renesas, Synopsys, Marvell, FPT Semi, Viettel	Ho Chi Minh City (HCMC), Ha Noi, and Da Nang	6,000 design engineers 2,000 support staff / quality assurance / admin (assuming 3 : 1 engineer-to-support mix)	65,000 total by 2030 (50,000 design engineers and proportional support)	Government goal is 50,000 engineers; total count extrapolates the same staffing mix.
Intel Vietnam	HCMC (Saigon Hi-Tech Park)	6,000 employees	n/a site already at full back-end capacity; future head-count expected to stay around this level barring a new fab	Largest Intel ATP site worldwide.
Amkor Technology Vietnam	Bac Ninh (Yen Phong)	1,200 employees	5,700 7,200 jobs once full Phase 1 ramp is complete in 2026	Environmental-impact filing shows tripling of capacity and a 5-6 times labour increase.
Hana Micron Vina	Bac Giang (Van Trung)	1,600 employees	4,000 jobs by 2025	Phase 2 will more than double current back-end workforce.

Table A2. Viet Nam' s existing semiconductor workforce and expansion target (continued)

Segment / facility	Province / city	Approximate current head-count* (mid-2025)	Expansion target** (announced estimation)	Notes
Other pipeline OSAT lines: Samsung Electro-Mechanics (FC-BGA), CT Semi, VDL…	Thai Nguyen, Binh Duong (under construction)	N/A, est. less than 200 (tool-install & pilot teams)	Low-thousands when mass-production starts (2027-28)	Workforce figures not yet disclosed; provincial filings indicate "several thousand" operators and engineers at full scale.
Total (design and ATP)		Approximately 14,000-17,000 people	85,000 by 2030	Current total sums rows above; 2030 figure aggregates published company build-out plans plus the national goal.

Note: World Bank staff compilation based on various official resources and announcements.

*Head-count includes everyone on the payroll – production operators, technicians, engineers, managers, quality, human resources (HR), finance, environmental health and safety (EHS), etc.

**Expansion target reflects the latest public commitments (EIA reports, company statements, or government targets). Figures are rounded to the nearest hundred because hiring ramps fluctuate month-to-month.

ANNEX 4. VIET NAM' S TALENT GAPS: THE ANALYSING FRAMEWORK AND SCENARIO MAPPING

A framework for analyzing four archetypal talent gaps

The framework for analyzing talent gaps in Viet Nam' s semiconductor industry is designed by benchmarking two main components: the demand for skills and the supply of talent across four scenarios – the current state (status quo) and three future-oriented scenarios. This analysis focuses on two segments where Viet Nam currently has a strong foothold and/or opportunities to upgrade in the global value chain (GVC): IC design and ATP/AP. Figure A1 provides a detailed presentation of this framework.

On the demand side, the analysis examines job requirements from leading semiconductor firms in each segment, with a focus on education and training levels, education majors, and skills. The skills requirements are categorized into technical skills, software capabilities such as AI/machine learning (ML), and professional "soft" skills. The deep dive into specific skills in demand is particularly focused on entry-level positions, including internships and roles requiring less than two years of experience, which are most relevant for university graduates. The list of semiconductor firms used for the analysis is presented in Table A3 and Figure A2.

On the supply side, we use data from the national labor force survey and university disclosures on annual enrollment by education level and major to analyze the current workforce stock and the flow of new graduates. For the stock, we focus on the workforce in the broader services and industries which cover semiconductor firms in Viet Nam. Specifically, ATP firms are included in the Manufacture of electronic components & boards industry, which encompasses the manufacture of semiconductors and other components for electronic applications. IC design firms are included in the Computer programming services, which involve writing, modifying, testing and supporting software. The list of semiconductor firms operating in Viet Nam under the Manufacture of electronic components & boards industry and the Computer programming services is provided in Table A4.

Figure A1. Overall framework for analyzing four archetypal talent gaps

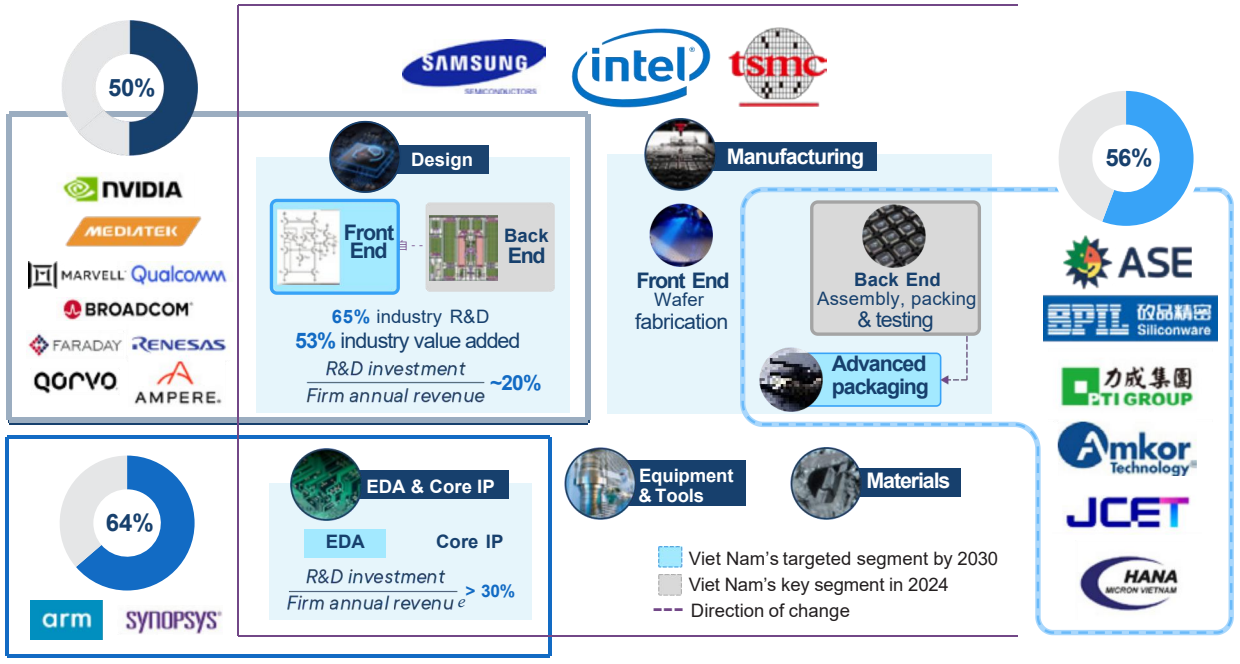
The gaps identified in our market-level analysis are corroborated by the findings from the industry assessment conducted by Nguyen, Tran, and Bergman (2025), which included in-depth interviews with Viet Nam' s leading semiconductor firms and industry insights. This convergence underscores the consistency and reliability of the insights gained.

Table A3. List of semiconductor firms used for talent gap analysis

Company	Country of headquarters	Market share of respective segment
Design		
NVIDIA	US	30%
Marvell	US	1%
MediaTek	Taiwan, China	4%
Qualcomm	US	9%
Broadcom	US	6%
Renesas	Japan	2%
Ampere Computing	US	1%
Faraday Technology	Taiwan, China	<1%
Qorvo, Inc.	US	<1%
IP & EDA		
ARM (Softbank)	United Kingdom	42%
Synopsys	US	22%

Company	Country of headquarters	Market share of respective segment
IDM		
Samsung	South Korea	
Intel	US	
Frontend manufacturing		
TSMC	Taiwan, China	
ATP		
Amkor Technology	US	16%
ASE Holdings (incl. Siliconware Precision Industries Co., Ltd. & ASE)	Taiwan, China	24%
JCET	China	10%
Powertech Technology Inc. (PTI)	Taiwan, China	6%
Hana Micron Vina	South Korea	

Figure A2. Semiconductor firms used for talent gap analysis



Sources for Figure A2 and Table A3: World Bank staff calculations based on market reports by Data Insights Market, Custom Market Insights, IPnest, SNS Insider and companies' annual reports and disclosure.

Note: (*) The total market share of each segment does not include that of Samsung, Intel, and TSMC, as these companies do not disclose revenue breakdowns by specific segments of the value chain. We also exclude the market shares of Renesas Electronics, Ampere Computing, Faraday Technology, and Qorvo, Inc., Hana Micron Vina from this calculation, as we only collected their job requirements in Viet Nam.

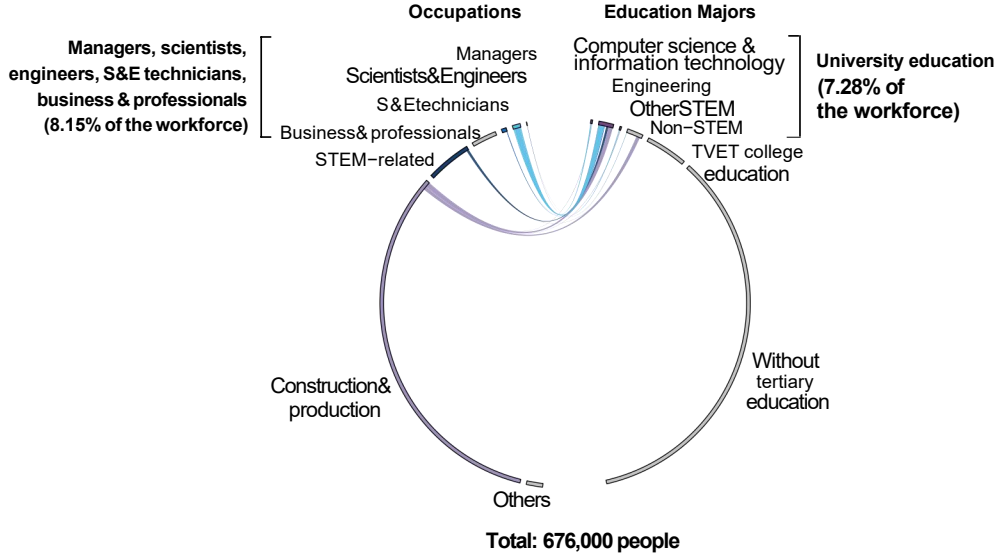
Table A4. Semiconductor-related service and industry and leading semiconductor firms in Viet Nam

Industry	Leading semiconductor firms in Viet Nam
Computer programming services (2610)	Toshiba Software Development Vietnam; Renesas Design Vietnam; Savarti; Uniquify Viet Nam; Faraday Technology Vietnam; CoAsia SEMI Vietnam; Synopsys Vietnam; Qorvo Vietnam; Dolphin Technology Vietnam Center; Sanei Hytechs Vietnam; BOS Semiconductors; Synapse Design Vietnam
Manufacture of electronic components & boards (6201)	Amkor Technology Vietnam; Intel Products Vietnam; On Semiconductor Vietnam; Hana Micron Vietnam

Source: World Bank staff compilation.

ANNEX 5. DEMAND FOR SKILLS IN VIET NAM AND FOREIGN MARKETS: SUPPLEMENTARY DATA TABLES

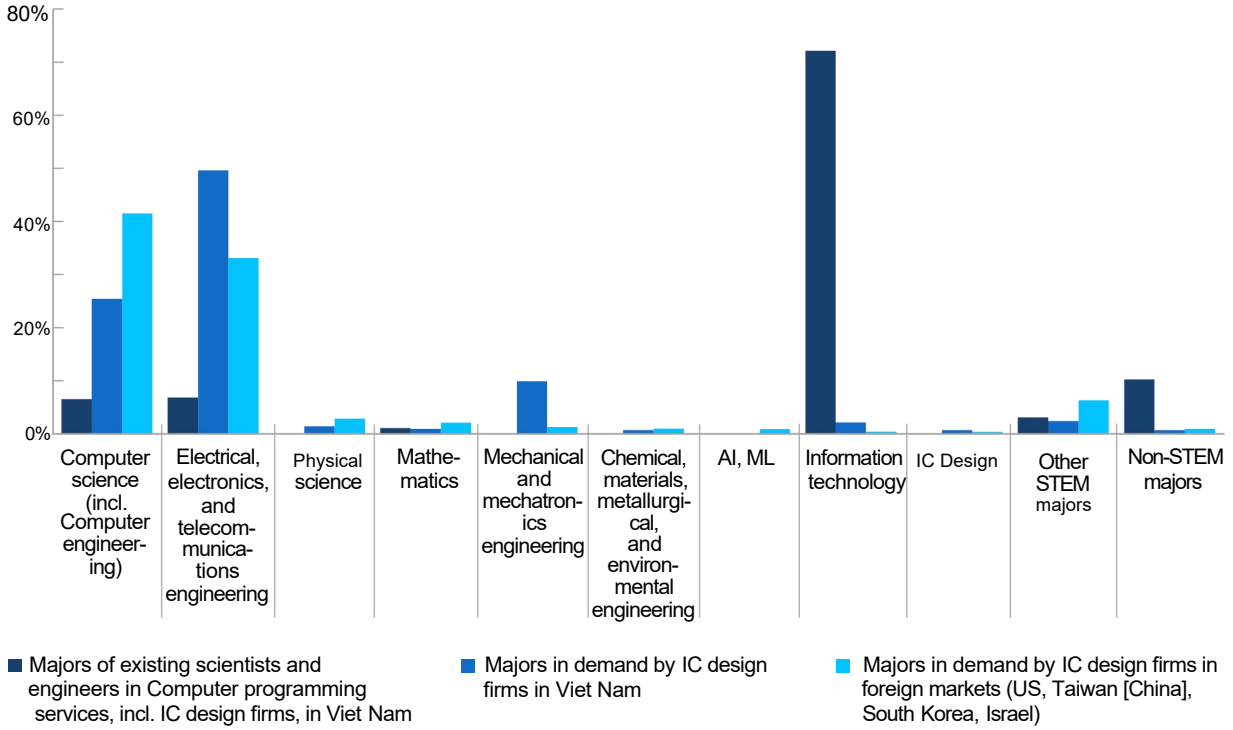
Figure A3. Occupations and majors of the existing workforce in Manufacture of electronic components & boards (incl. ATP firms)



Source: World Bank staff calculations based on LFS 2023.

Note: Sample include female workers aged 20-55 and male workers aged 20-60. STEM-related occupations consist of health occupations; architects, planners, surveyors, and designers; and occupations requiring high STEM expertise but not a bachelor's degree for entry.

Figure A4. Majors of existing scientists and engineers in Computer programmingservices vs. demand by IC design firms in Viet Nam and foreign markets



Sources: World Bank staff calculations based on LFS 2023, job requirements from IC design firms operating in Viet Nam and foreign markets.

Note: Job requirement sample excludes non-technical, corporate support positions (e.g., roles in sales, purchases, procurement, legal, compliance, accounting & finance, HR, and administration).

Table A5. Demand for specific skills of workers with more than 2 years of experience by IC design firms

Skills Groups	Skills	By IC design firms in Viet Nam (mostly back-end design)	By IC design firms in foreign markets (mostly front-end design)
Technical Skills	Digital Design	Fundamental digital logic skills, RTL coding, FPGA design, basic familiarity with Verilog, VHDL	Advanced ASIC/RTL design, complex digital circuits, deep RTL optimization, SystemVerilog, synthesis, timing closure, multi-threaded designs
	Analog & Mixed-Signal Design	Basic transistor-level analog design, basic PLL circuits, understanding of basic mixed-signal circuits	Extensive analog design, comprehensive mixed-signal integration, advanced PHY design, advanced CMOS design (deep sub-micron nodes), signal integrity
	System Architecture	Basic understanding of processor and memory architecture, limited exposure to system-level integration	Strong emphasis on advanced system-level architecture
	Fabrication & Process	Basic semiconductor fabrication process knowledge	Deep understanding of advanced processes, reliability analysis, advanced packaging, fabrication reliability
	Verification & Testing	Basic transistor-level simulations, fundamental circuit-level verification	Advanced verification methodologies
Tool Skills	EDA/CAD Tools	Basic familiarity with Cadence, Synopsys tools, basic circuit simulators (HSpice, ModelSim, Spectre)	Advanced proficiency (Synopsys Fusion Compiler, Cadence Innovus/Genus/Virtuoso, Calibre, PrimeTime, Voltus, FPGA emulation, debugging tools, static timing, EM/IR-drop analysis)
	Scripting & Automation	Basic scripting skills (Python, TCL, Perl), basic Linux usage	Advanced scripting/programming (Python, Perl, TCL, Unix Shell, Makefile), extensive Linux proficiency, CI/CD flow automation, design flow automation
	PCB Tools	Limited PCB design skills; basic knowledge of layout entry tools	Advanced PCB design skills, high-speed PCB design, signal integrity, power integrity, EMC compliance, detailed layout verification
AI/ML Skills	Data Handling & Automation	Basic Python scripting skills for general data handling	Advanced deep-learning models, generative AI, AI performance profiling and optimization
	AI Applications	N/A	Extensive applications (computer vision, image processing, real-time decision algorithms, AI model deployment, optimization for hardware accelerators)
	AI Frameworks & Tools	N/A	Proficiency with AI frameworks (TensorFlow, PyTorch, ONNX, MLIR, TVM)
Language & Soft Skills	Language Proficiency	Moderate English proficiency; mainly reading and writing, basic technical communication skills	Advanced English proficiency (technical documentation, technical presentations, fluent verbal and written communication)
	Teamwork & Collaboration	Good teamwork, interpersonal skills, self-motivated, ability to collaborate effectively	Advanced teamwork and collaboration (cross-functional, international teams), strong emphasis on coordination and effective communication
	Work Flexibility' Mindset' Leadership	General adaptability, proactive learning approach, basic analytical skills	High adaptability and independence, proactive learning and initiative-taking, strong analytical mindset, advanced problem-solving, excellent project management skills, strong leadership, strategic thinking, prioritization skills

Sources: World Bank staff analysis based on job requirements from IC design firms (Synopsys Inc., Marvell Technology, Nvidia Corporation, MediaTek Inc., Renesas Electronics, Broadcom Inc., Qualcomm Inc., Ampere Computing, Faraday Technology, and Qorvo, Inc.); IP firms (Arm Holdings plc), and IC design job requirements from Intel, Samsung Semiconductor, and TSMC, accessed in March-April 2025. Data for Renesas Electronics, Ampere Computing, Faraday Technology, and Qorvo, Inc. includes only Viet Nam postings.

Table A6. Demand for specific skills of workers with more than 2 years of experience by ATP/advanced packaging firms

Skills Groups	Skills	By ATP firms in Viet Nam	By ATP/AP firms in foreign markets (China, Taiwan [China], Malaysia)
Technical skills	Electronics/ Electrical	SMT lines, basic electronics maintenance, PCB assembly, EMS experience	Advanced IC packaging (flip-chip, TSV, Hybrid Bonding, RDL) Semiconductor-specific processes (die bonding, wire bonding, lithography, electroplating, wafer-level packaging)
	Quality Management	Basic QC standards, familiarity with ISO/IATF16949	Advanced standards (ISO9000, TS16949, JEDEC, VDA6.3, automotive quality) Statistical tools (SPC, DOE, Six Sigma Black Belt, FMEA, 8D)
	Environmental and Safety Systems	Basic knowledge of HVAC, wastewater treatment, chemical safety	Detailed environmental control systems (ultrapure water, air pollution control, compliance with Occupational Safety & Health Act)
	Mechanical Engineering	General equipment operation and maintenance, basic mechanical skills	Advanced mechanical skills, clean room facility management, detailed knowledge in piping, duct design, HVAC, and electromechanical projects
	IT Infrastructure	General knowledge of Linux/Unix, Windows Servers	Advanced IT skills: NAS/SAN storage, Hyper-V clustering, security/firewalls, system compliance (ISO27001/22301), advanced certifications (CCNA/CCNP)
	Design Engineering	Basic CAD (AutoCAD 2D/3D), knowledge of general assembly processes	Advanced IC package design (FCBGA, fcCSP) Proficient with design software (Cadence, Mentor Expedition) Simulation tools (Ansys, COMSOL)
AI, ML	AI, ML	N/A	Data analysis, ML, deep learning, computer vision (TensorFlow, OpenCV, Cognex, Halcon, Keras)
Tool skills	MS Office	MS Office	MS Office
	CAD Tools	Basic proficiency in AutoCAD (2D, 3D)	Advanced proficiency required (Cadence, Mentor Expedition, advanced AutoCAD use for packaging design)
	Programming & Automation Tools	Basic programming (Excel Macro, Python, basic C#, .NET)	Advanced proficiency required (Python, C#, Java, SQL scripting, T-SQL, P/L SQL, PowerShell scripting)
	Measurement & Testing Tools	Basic lab equipment (oscilloscope, spectrum analyzer, network analyzer)- Automated Test Equipment (basic)	Advanced ATE systems (Advantest, Teradyne) Specialized metrology equipment (X-ray, SEM, FIB)
	Control Systems	Basic understanding of SCADA, Central Control Room operation	Advanced control systems knowledge
Language & soft skills	Language	English proficiency required	Strong, standardized English proficiency
	Soft Skills	Interpersonal skills, effective teamwork, basic management skills	Advanced soft skills: teamwork, global communication, coordination, leadership, cross-cultural management, strong analytical/problem-solving skills
	Shift Flexibility & Mobility	Basic flexibility, occasional international training opportunities	High flexibility, frequent international travel, willingness for relocation or extensive international assignments

Sources: World Bank staff analysis based on job requirements from ATP/advanced packaging firms (Amkor Technology, Siliconware Precision Industries, Advanced Semiconductor Engineering, Powertech Technology Inc., JCET Group, and Hana Micron Vina) and ATP/advanced packaging job requirements from TSMC and Intel, accessed in March-April 2025.

ANNEX 6. SUMMARY OF VIET NAM'S POLICY LANDSCAPE IN 2025

Annex 6.1. Viet Nam's strategy for "Semiconductor Industry Development Strategy to 2030 and Vision for 2050"

In September 2024, the Prime Minister approved Viet Nam's "Semiconductor Industry Development Strategy to 2030 and Vision for 2050" (the Strategy) and the "Workforce Development for the Semiconductor Industry by 2030, with a Vision to 2050" program (the Program). These initiatives aim to position Viet Nam as a key player in the global semiconductor value chain.

The development formula highlighted in the Strategy is C = SET + 1, where:

C: Chip,

S: Specialized (chips),

E: Electronics (industry),

T: Talent (Talents, Workforce), and

+ 1: Viet Nam (Viet Nam will strive to become a new and safe destination of the global semiconductor value chain).

Positioning of workforce development in the national industry strategy: Workforce is the core pillar of the Strategy and is identified as the foundation for the formation of the semiconductor industry in Viet Nam. Developing Viet Nam as a center for global workforce across all processes of the semiconductor value chain is the first step of the Strategy. A high-quality workforce will generate competitive advantages for Viet Nam to attract foreign investment.

The Strategy is divided into three phases: phase I during 2024-2030, phase II during 2030-2040, and phase III during 2040-2050. The objectives of each phase are presented in Table A7 below.

The Strategy also includes five focused projects, schemes, and task areas:

- Specialized Chip Development: Research and develop core technologies for specialized chips, particularly in AI and IoT; build a domestic semiconductor ecosystem that connects with ecosystems in strategically partnered countries.
- Electronics Industry Development: Support the development of next-generation electronics integrated with specialized chips; prioritize domestic products; and promote large domestic electronics enterprises to become multinational companies.
- Talent Attraction and Workforce Development: Adopt and implement the workforce development program (focusing on reskilling, upskilling, and transfer programs); invest in both infrastructure and non-infrastructure activities of training and research centers; develop mechanisms and policies to attract talents; and promote national cooperation in training and supplying high-quality workforce.
- Investment Attraction: Develop policies to attract high-tech foreign direct investment (FDI) firms and one-stop shop for investment projects in the semiconductor and electronics industries; develop an investment support fund; develop prioritized policies for foreign companies that conduct R&D in Viet Nam, utilize domestic supporting industries, or form joint ventures; invest in infrastructure supporting the development of semiconductor fabrication plants.
- Environmental and International Collaboration: Promote green manufacturing and safe waste disposal; and expand international collaborations.

Table A7. Three phases of developing the Viet Nam' s semiconductor and electronics industries

	Phase I (2024-2030)	Phase II (2030-2040)	Phase III (2040-2050)
General objectives	• Selective attraction of FDI • Becoming a global semiconductor workforce center • Growing fundamental capacity in all processes (from research, design, and fabrication to ATP)	• Becoming a global semiconductor and electronics center • Strong linkages between FDI and domestic firms	Becoming a leading country in the semiconductor and electronics industries
Workforce	• 50,000+ engineers and experts with university degrees and higher[53] • 1,300 semiconductor training on trainers in research institutions, universities	100,000+ engineers and experts with university degrees and higher	Workforce structure and size that meets the development of the demand-side
Training and R&D labs[54]	• 04 national-level shared semiconductor labs • 18 institutional-level semiconductor labs		
Firms and factories	• 100 semiconductor design firms • 01 small-scale semiconductor fabrication plant • 10 ATP factories • Developing some specialized semiconductor products	• 200 semiconductor design firms • 02 semiconductor fabrication plants • 15 ATP factories • Autonomy on technologies in the design and fabrication process	• 300 semiconductor design firms • 03 semiconductor fabrication plants • 20 ATP factories • Autonomy in R&D
Semiconductor industry	• Revenues: US$25+ billion • Domestic value added: 10-15%	• Revenues: US$50+ billion • Domestic value added: 15-20%	• Revenues: US$100+ billion • Domestic value added: 20-25%
Electronics and electrical equipment industry	• Revenues: US$225+ billion • Domestic value added: 10-15%	• Revenues: US$485+ billion • Domestic value added: 15-20%	• Revenues: US$1,045+ billion • Domestic value added: 20-25%
Semiconductor industry ecosystem			Establishing a self-sufficient semiconductor industry ecosystem in Viet Nam, positioning the country as a leader in specific processes, segments of the value chain

[53] This target is further broken down in the workforce development program as follows: (i) by qualification – 42,000 engineers and university graduates, 7,500 Master degree holders, and 500 PhD holders; (ii) by value chain segment – 15,000 in the design segment and 35,000 in the ATP segment, and at least 5,000 AI experts.

[54] These targets are set in the Program. 04 national-level labs are planned at National Innovation Center (NIC), Vietnam National University Ho Chi Minh City (VNUHCM), Vietnam National University, Hanoi (VNUHN), Da Nang city. The lab at NIC (in collaboration with Hanoi University of Science and Technology) focuses on design and ATP segments; training and incubation activities, entrepreneurship, and AI applications. The lab atVNUHN focuses on manufacturing segment. The lab atVNUHCM serves all segments from design, manufacturing to ATP. The lab in Da Nang city focuses on design and testing segment.

Annex 6.2. SeIected science, technoIogy, innovation (STI) poIicies

Viet Nam'sIeadership has recentIy approved a series of instruments that set the stage for transformative change in the STI and higher education Iandscape. These milestones establish a high-level vision, legal mandates for reform, and new funding mechanisms:

- PoIitburo ResoIution 57-NQ/TW (22 December 2024): This Party Resolution defines a bold vision for STI and the digital economy through 2030 and 2045. It calls for "đột phá" (breakthrough) development of science, technology, innovation and national digital transformation, considering these as "prerequisites and the best opportunity" for Viet Nam to become a high-income, powerful country. Resolution 57-NQ/TW sets specific targets – e.g., By 2030, Viet Nam should be in the top 3 ASEAN countries in digital competitiveness and innovation, and the digital economy should contribute at least 30 percent of Gross Domestic Product (GDP). By 2045, Viet Nam s digital economy is envisioned at >50 percent of GDP. It also mandates strengthening human capital in key technology areas (e.g., semiconductors, AI, big data, IoT, etc) and increasing R&D investment to 2 percent of GDP. This high-level Resolution provides strategic direction and political backing for subsequent laws and programs.

- NationaI AssembIy (NA) ResoIution 193/2025/QH15 (19 February 2025): This Resolution, passed by the 15th NA, authorizes the piloting of special mechanisms and policies to create breakthrough development in science, technology, innovation, and national digital transformation. Resolution 193/2025/QH15 was enacted specifically to institutionalize the mandates of Resolution 57-NQ/TW into law. It acknowledges persistent "bottlenecks" in Viet Nam s innovation system and permits controlled policy experiments during 2025 2030 in order to unblock these. Key provisions of Resolution 193 include: (a) granting greater autonomy and incentive structures for research institutions and higher education establishments, especially to commercialize research; (b) new financing models for R&D (e.g., lump-sum funding grants, tax incentives for innovation); (c) streamlined procedures in areas like procurement and talent recruitment for STI projects; and (d) targeted support to strategic technology projects notably, the Resolution explicitly mentions facilitating the first Vietnamese semiconductor fabrication plant and other strategic digital infrastructure (like 5G networks and undersea cables) through special incentives. Resolution 193 took effect in mid-2025 and required the GoV to issue detailed guidelines for implementation.

- Government Decree 88/2025/NĐ-CP (13 April 2025): In response to Resolution 193, the GoV promulgated Decree 88 to detaiI and guide the impIementation of the authorized special STI mechanisms. Decree 88/2025 is a comprehensive instrument that operationalizes the pilot policies. Key features include:

  - Facilitating Research Commercialization: Public-sector scientists, university faculty, and research institute staff are now allowed to establish or participate in start-up enterprises based on their research, with a protective "safe harbor." Under Decree 88, if a public university or research institute spins off a company, its staff can be seconded to work at the enterprise with approval. Their public sector position, salary, and benefits are preserved during the assignment, and they are guaranteed a suitable job on return. This removes a major disincentive for faculty entrepreneurship they no longer risk their careers by engaging in commercialization. It effectively provides a "dual appointment" mechanism and safety net for innovators in academia, as envisioned by Resolution 193.

  - Encouraging Risk-Taking in R&D: Decree 88 stipulates that if a state-funded R&D project does not achieve its intended results, the implementing institution will not have to refund the used funding, as long as the project was carried out in accordance with approved objectives and procedures. Only unspent funds or funds misused outside the project scope must be returned. This is a pivotal shift from past practices it acknowledges the experimental nature of research and encourages ambitious, innovative projects by removing the fear of penalty for failure. Researchers can pursue breakthrough ideas without the same bureaucratic risk aversion.

- Flexible Funding and Procurement: In line with Resolution 193's mandate, the decree implements "khoán chi" (lump-sum funding) for approved S&T tasks, meaning research teams are given flexibility to use funds toward agreed outputs instead of rigid line-item controls. It also allows expedited procurement methods (e.g., direct contracting) for specialized R&D equipment and services as needed for the pilot projects, speeding up implementation.

- Talent and Tax Incentives: Decree 88 elaborates incentives for high-tech enterprises and projects. For instance, an enterprise investing in Viet Nam's first semiconductor R&D and production facility is permitted to allocate up to 20 percent of its pre-tax income to its science and technology fund (double the usual cap) to reinvest in the project. Moreover, state-owned enterprises (100 percent state capital) that invest in designated high-tech projects (like 5G infrastructure, international fiber-optic cables, orthe semiconductor fab) will not have those project expenditures count against their financial performance evaluations – any accounting losses from such strategic projects can be excluded when assessing the state owned enterprises' profit/loss for ranking purposes. These measures, guided by Resolution 193, incentivize firms to pour resources into critical innovative projects without fear of short-term financial drawbacks.

- Digital Transformation Measures: A separate chapter in Decree 88 addresses national digital transformation activities. It covers support for digital platform development, use of open data, and public-private partnerships in digital services, complementing the STI policies. For example, it encourages businesses to invest in digital technology adoption by recognizing all innovation-related expenditures as deductible for corporate income tax purposes.

- Investment Support Fund (ISF) for High-Tech and R&D (Decree 182/2024/NĐ-CP, 31 December 2024): Alongside the above, the GoV established a new ISF to catalyze high-tech industry projects and related workforce development. Issued at the end of 2024, Decree 182/2024/NĐ-CP creates a fund that offers co-financing grants to eligible enterprises in advanced technology sectors. This policy is a timely innovation, partly to maintain Viet Nam's investment appeal in the era of global minimum tax reforms. Key features include: up to 50 percent subsidy of a project's initial R&D center investment cost in semiconductor or AI sectors, and up to 50 percent of annual expenditures on training and workforce development for Vietnamese employees in high-tech projects. The fund targets large-scale investments – for example, a semiconductor manufacturing or design project must have a capital size above a threshold (e.g., VND 6,000+ billion for chip-related projects) to qualify. Supported beneficiaries include certified high-tech enterprises, firms producing high-tech products, firms applying high-tech in production, and those building R&D centers.

ANNEX 7. SUMMARY OF THE SWOT ANALYSIS

Strengths:

- Strong government commitment and policy momentum (e.g., Politburo Resolutions 57 and 68).
- An established ATP manufacturing base with global players like Intel and Amkor, providing a platform to move up the semiconductor value chain.
- Growing science, technology, engineering, and mathematics (STEM) talent pipeline and improving university rankings.
- Competitive labor costs and a young workforce.
- New IC design training programs modeled on international benchmarks, and emerging university–industry partnerships (creating entry points for co-investment).

Weaknesses:

- Limited postgraduate programs and output (very few Master's/PhD graduates in semiconductor-related fields).
- Inconsistent infrastructure for teaching, research and innovation; limited access to industry-grade electronic design automation (EDA) tools (some labs are well-equipped, but many are small or outdated – key facilities like cleanrooms and advanced prototyping labs remain in short supply).
- Fragmented funding and weak incentives for faculty to pursue R&D (research grants are modest; academic promotion places little emphasis on patents or industry collaboration).
- Acute shortage of specialized talent, especially in front-end chip design and advanced packaging.
- Low female representation in STEM and in semiconductor engineering roles.

Opportunities:

- Surging global semiconductor demand – driven by AI, electrification, and digital transformation – creates space for new entrants and "talent hubs."
- Global supply chain diversification (China+1 strategies) opens a window for Viet Nam to attract investment and leapfrog into advanced packaging and front-end design niches.
- Proven public-private partnership (PPP) models can be adapted to establish national semiconductor hubs and shared R&D infrastructure (leveraging both public funds and industry co-investment).
- Strong investor momentum can be harnessed by strengthening IP frameworks and commercialization pathways in universities and the wider ecosystem.
- Opportunity to engage the Vietnamese diaspora and forge new international partnerships for training, research, and innovation (to import expertise and expand capacity quickly).

Threats:

- Brain drain of top talent due to better opportunities abroad (the US, Europe, other Asian tech hubs).
- High volatility and geopolitical complexity in the semiconductor sector (e.g., export controls, trade tensions) adding uncertainty to long-term investments – on top of the industry's inherent cyclical risks.

特别提醒

行业交流分享群

分享：可获取人资行业的报告、方案及其他学习资源，上新群内通知

交流：求职、找人、找资源、找供应商

客服

交流群

免责声明

第三方声明：本报告所有内容（数据/观点/结论）整理于网络公开渠道，均不代表我司立场，我司不承担其准确性、完整性担保责任。

侵权处理承诺：如报告内容涉嫌侵权，请立即联系客服微信，我司将在核实后第一时间清理相关内容并配合处理

- An aging population beyond 2035 will begin reducing Viet Nam' s youth labor pool, potentially eroding its demographic advantage.
- Risk of underfunding or slow implementation of core initiatives – ambitions may falter if budget allocations or execution lag.
- Hesitation from the private sector in co-investing or engaging (e.g., if firms doubt the quality of local research or talent), which could undermine public efforts.